PCN Number:	20130423000	PCN Date: 05/01/2013
Title: DM814x, DM	812X, DRA64X, AM387x, DM814xSEC Data	Sheet
Customer Contact:	PCN Manager Phone: +1(214) 480-603	7 Dept: Quality Services
Change Type:		
	Electrical Specification	
Description of Chang	PCN Details	
The product datasheet sequenceing.	(s) is being updated to change to device por	wer-up/down supply
The following change h datasheet links provide	nistory provides further details. These chang ed.	es may be reviewed at the
Digital Medi	814x DaVinci™ a Processors isions 3.0, 2.1	
Shicon Kev	510115 5.0, 2.1	
Silicon E	rrata	
		AS TRUMENTS
	Literature Number: SPRZ343C September 2011-Revised March 2013	

This silicon errata revision history highlights the technical changes made to the SPRZ343A revision to make it an SPRZ343B revision, as well as the technical changes made to the SPRZ343B revision to make it an SPRZ343C revision.

Scope: Applicable updates relating to the TMS320DM814x devices have been incorporated.

DM814x Revision History

evision C (Silico	on Revision 3.0) Changes below:
Global	Added Silicon Revision 3.0 device-specific data
Section 1.2	Package Symbolization and Revision Identification:
Section 1.2	Updated/Changed "Figure 1 shows" paragraph
Figure 1	Example, Device Revision Codes:
Figure 1	 Updated figure to show an example of silicon revision 3.0 ("C" or "S")
Table 1	TMS320DM814x Device Revision Codes:
Table 1	Added Silicon Revision 3.0 ("C") device-specific data
Section 2	Silicon Revision 3.0 Usage Notes and Known Design Exceptions to Functional Specifications:
Section 2	Added new section
Section 2.1	Usage Notes for Silicon Revision 3.0:
Section 2.1	Added new section
	Moved the following 2.1 Usage Notes to this new section:
	 Section 2.1.1, DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit
	 Section 2.1.2, Some PLLs Only Support Even M2 Post Dividers
	 Section 2.1.3, DDR2 and DDR3 Requires Software Leveling
Section 2.2	Silicon Revision 3.0 Known Design Exceptions to Functional Specifications:
	Added new section
	Moved all other 2.1 Advisories to this section except for these:
	•
	 Advisory 2.1.27, SATA: Unable to Operate Both SATA and VOUT0 Without SATA Locking Up Advisory 2.1.28, SATA: Link Establishment Fails With SATA GEN3 Capable Targets
	Advisory 2.1.51,HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After
	HDVPSS Reset or VIP Client Abort Causes Lockup
	 Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing
	Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring
	 Advisory 2.1.68,DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power-On Hours May Occur if the Input Receiver is Disabled
Section 3.1	Usage Notes for Silicon Revision 2.1:
	 Updated/Changed "Silicon revision 2.1 applicable usage notes" paragraph
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:
	 Updated/Changed "This is a list of the device revision 2.1 known" paragraph
	 Added Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing
	Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring
	tory SPRZ343C-September 2011-Revised Marc

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DM814x Revision History

SEE	ADDITIONS/MODIFICATIONS/DELETIONS	
Revision B (Silic	n Revision 2.1) Changes below:	
Global	Updated/Changed "DEMMU" to "System MMU"	
	Updated/Changed "Digital Media Processors" to "Video Processors"	
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:	
	Updated/Changed the Data Manual Doc Titles	
	Advisory 2.1.25, System DEMMU May Hang When Used in Table-Walk Mode:	
	Updated/Changed the System MMU Entries (Entry 1 through Entry 7) code in the System MMU Lockdown Example.	
	Added the following Advisories to this section:	
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup 	
	 Advisory 2.1.54, VPDMA Line Limit Feature: Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields in Memory 	
	 Advisory 2.1.55, HPVPSS VIP Inline Color Space Converter (CSC): In Interlaced Embedded or Discrete Sync Mode, Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields In Memory 	
	 Advisory 2.1.58, HDVPSS: HDVPSS VIP Reset Sequence is Occasionally Unsuccessful if VPDMA is Writing Output Descriptors for VIP Captured Data 	
	 Advisory 2.1.60, HDVPSS: Occasionally, During Connect/Disconnect and When Line or Width Limit Feature Not Used, Any Memory Areas Can Be Overwritten 	
	 Advisory 2.1.82, HDVPSS: Discrete Sync Interlaced Output Mode: Vertical Sync Output For Odd Fields May Not Correctly Detect Video Signal 	
	 Advisory 2.1.63, HDVPSS: VIP Single-Channel Capture Using Tiled Output Can Lead To VIP Lockup if Connect/Disconnect Events Occur 	
	 Advisory 2.1.66, PCI Express (PCIe): PCIe Boot Fails When Connected to Some PCs 	
	 Advisory 2.1.68, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth 	
	 Advisory 2.1.70, USB: A USB Device that Responds to a Spurious Invalid Short Packet may Lock up the Bus Advisory 2.1.71, ROMCODE: PCIe Boot is Unstable 	
	Advisory 2.1.72, ROMCODE: ROM Code Does Not Support Booting from eMMC Devices of Size 4GB or More	
	 Advisory 2.1.76, UART: Extra Assertion of the FIFO Transmit DMA Request, UARTi_DMA_TX 	
	 Advisory 2.1.79, EDMA: TC0 and TC1 Read Accesses Always Use Physical Address 	
	Advisory 2.1.80, Power Sequencing: CVDD versus CVDD_*	
	Advisory 2.1.81, Power Sequencing: 3.3V DVDD* versus VDDA_1P8	
	Advisory 2.1.82, Power Sequencing: DVDD_DDR[x] versus 3.3V DVDD* Supplies	
	 Advisory 2.1.85, EMAC and Switch Subsystem: Reset Isolation Feature is Not Supported Advisory 2.1.87, Cantral Madula, Bin Canfinguration (BINCNTL), 2.2 V Mada Constitution in Research 	
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power- On Hours May Occur if the Input Receiver is Disabled 	
	 Advisory 2.1.88, Control Module, Pin Configuration (PINCNTLx): ROM Modifies Bit 19 	



This silicon errata revision history highlights the technical changes made to the SPRZ385 revision to make it an SPRZ385A revision, as well as the technical changes made to the SPRZ385A revision to make it an SPRZ385B revision.

Scope: Applicable updates relating to the TMS320DM812x devices have been incorporated.

DM812x Revision History

Section 1.2 Package · Upp Figure 1 Example · Upp Table 1 TMS320 · Add Section 2 Silicon R Added n Section 2.1 Usage N Added n Moved ti · Sec · Sec · Sec · Sec · Section 2.2 Silicon R Added n Moved ti · Sec ·	Section Revision 3.0 device-specific data Section Revision 3.0 device-specific data Section Revision and Revision Identification: dated/Changed "Figure 1 shows" paragraph A. Device Revision Codes: dated figure to show an example of silicon revision 3.0 ("S") IDM8127 Device Revision Codes: dated Silicon Revision 3.0 ("C") device-specific data Revision 3.0 Usage Notes and Known Design Exceptions to Functional Specifications: lew section Revision Revision 3.0: Revision 2.1 Usage Notes to this <i>new</i> section: ction 2.1.1, DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit ction 2.1.2, Some PLLs Only Support Even M2 Post Dividers ction 3.0 Known Design Exceptions to Functional Specifications: lew section all other 2.1 Advisories to this section except for these: livisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After VPSS Reset or VIP Client Abort Causes Lockup visory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing gle-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring
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Section 3.1 Usage N • Upo Section 3.2 Silicon R • Upo • Add Sin	visory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction
Section 3.2 Silicon R • Upo • Add Sin	Power-On Hours May Occur if the Input Receiver is Disabled
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Section 3.2 Silicon R Upo Add	lotes for Silicon Revision 2.1:
• Upo • Ado Sin	dated/Changed "Silicon revision 2.1 applicable usage notes" paragraph
- Upo - Ado Sin	Revision 2.1 Known Design Exceptions to Functional Specifications:
Sin	dated/Changed "This is a list of the device revision 2.1 known" paragraph
	ded Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing
Ser	gle-Channel Capture,
I	nding Tiled Data to DDR and Connect/Disconnect Events are Occurring
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Revision History	SPRZ385B-June 2012-Revised March

000	DM812x Revision History (continued)
SEE	ADDITIONS/MODIFICATIONS/DELETIONS on Revision 2.1) Changes below:
Global	Updated/Changed "DEMMU" to "System MMU"
	Updated/Changed "Digital Media Processors" to "Video Processors"
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:
	Advisory 2.1.25, System DEMMU May Hang When Used in Table-Walk Mode:
	 Updated/Changed the System MMU Entries (Entry 1 through Entry 7) code in the System MMU Lockdown Example.
	Added the following Advisories to this section:
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup
	 Advisory 2.1.54, VPDMA Line Limit Feature: Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields in Memory
	 Advisory 2.1.55, HPVPSS VIP Inline Color Space Converter (CSC): In Interlaced Embedded or Discrete Sync Mode, Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields In Memory
	 Advisory 2.1.58, HDVPSS: HDVPSS VIP Reset Sequence is Occasionally Unsuccessful if VPDMA is Writing Output Descriptors for VIP Captured Data
	 Advisory 2.1.80, HDVPSS: Occasionally, During Connect/Disconnect and When Line or Width Limit Feature Not Used, Any Memory Areas Can Be Overwritten
	 Advisory 2.1.82, HDVPSS: Discrete Sync Interlaced Output Mode: Vertical Sync Output For Odd Fields May Not Correctly Detect Video Signal
	 Advisory 2.1.63, HDVPSS: VIP Single-Channel Capture Using Tiled Output Can Lead To VIP Lockup if Connect/Disconnect Events Occur
	 Advisory 2.1.68, PCI Express (PCIe): PCIe Boot Fails When Connected to Some PCs
	 Advisory 2.1.88, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth
	· Advisory 2.1.70, USB: A USB Device that Responds to a Spurious Invalid Short Packet may Lock up the Bus
	Advisory 2.1.71, ROMCODE: PCIe Boot is Unstable
	Advisory 2.1.72, ROMCODE: ROM Code Does Not Support Booting from eMMC Devices of Size 4GB or More
	 Advisory 2.1.76, UART: Extra Assertion of the FIFO Transmit DMA Request, UARTi_DMA_TX
	 Advisory 2.1.79, EDMA: TC0 and TC1 Read Accesses Always Use Physical Address
	 Advisory 2.1.80, Power Sequencing: CVDD versus CVDD_*
	 Advisory 2.1.81, Power Sequencing: 3.3V DVDD* versus VDDA_1P8
	 Advisory 2.1.82, Power Sequencing: DVDD_DDR[x] versus 3.3V DVDD* Supplies
	 Advisory 2.1.85, EMAC and Switch Subsystem: Reset Isolation Feature is Not Supported
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power- On Hours May Occur if the Input Receiver is Disabled
	 Advisory 2.1.88, Control Module, Pin Configuration (PINCNTLx): ROM Modifies Bit 19



This silicon errata revision history highlights the technical changes made to the SPRZ346 revision to make it an SPRZ346A revision, as well as the technical changes made to the SPRZ346A revision to make it an SPRZ346B revision.

Scope: Applicable updates relating to the DRA64x/DRA65x devices have been incorporated.

DRA64x/DRA65x Revision History

levision B (Silico	ADDITIONS/MODIFICATIONS/DELETIONS	
	Revision B (Silicon Revision 3.0) Changes below:	
Global	Added Silicon Revision 3.0 device-specific data	
Section 1.2	Package Symbolization and Revision Identification:	
	Updated/Changed "Figure 1 shows" paragraph	
Figure 1	Example, Device Revision Codes:	
	 Updated figure to show an example of silicon revision 3.0 ("C") 	
Table 1	DRA64x/DRA65x Device Revision Codes:	
	 Added Silicon Revision 3.0 ("C") device-specific data 	
Section 2	Silicon Revision 3.0 Usage Notes and Known Design Exceptions to Functional Specifications:	
	Added new section	
Section 2.1	Usage Notes for Silicon Revision 3.0:	
	Added new section	
	Moved the following 2.1 and earlier Usage Notes to this new section:	
	 Section 2.1.1, DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit 	
	 Section 2.1.2, Some PLLs Only Support Even M2 Post Dividers 	
	 Section 2.1.3, DDR2 and DDR3 Requires Software Leveling 	
Section 2.2	Silicon Revision 3.0 Known Design Exceptions to Functional Specifications:	
	Added new section	
	Moved all other 2.1 and earlier Advisories to this section except for these:	
	•	
	 Advisory 2.1.27, SATA: Unable to Operate Both SATA and VOUT0 Without SATA Locking Up 	
	 Advisory 2.1.28, SATA: Link Establishment Fails With SATA GEN3 Capable Targets 	
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup 	
	 Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring 	
	 Advisory 2.1.68, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth 	
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power-On Hours May Occur if the Input Receiver is Disabled 	
Section 3.1	Usage Notes for Silicon Revision 2.1:	
	 Updated/Changed "Silicon revision 2.1 applicable usage notes" paragraph 	
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:	
	 Updated/Changed "This is a list of the device revision 2.1 known" paragraph 	
	 Added Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing 	
	Single-Channel Capture,	
	Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring	

SPRZ346B-February 2012-Revised March 2013 Submit Documentation Feedback

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Revision History 71

DRA64x/DRA65x Revision History

SEE	ADDITIONS/MODIFICATIONS/DELETIONS	
Revision A (Silico	n Revision 2.1) Changes below:	
Global	Updated/Changed "DEMMU" to "System MMU"	
	Updated/Changed "Digital Media Processors" to "Video Processors"	
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:	
	Updated/Changed the Data Manual Doc Titles	
	Advisory 2.1.25, System DEMMU May Hang When Used in Table-Walk Mode:	
	 Updated/Changed the System MMU Entries (Entry 1 through Entry 7) code in the System MMU Lockdown Example. 	
	Added the following Advisories to this section:	
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup 	
	 Advisory 2.1.54, VPDMA Line Limit Feature: Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields in Memory 	
	 Advisory 2.1.55, HPVPSS VIP Inline Color Space Converter (CSC): In Interlaced Embedded or Discrete Sync Mode, Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields In Memory 	
	 Advisory 2.1.58, HDVPSS: HDVPSS VIP Reset Sequence is Occasionally Unsuccessful if VPDMA is Writing Output Descriptors for VIP Captured Data 	
	 Advisory 2.1.60, HDVPSS: Occasionally, During Connect/Disconnect and When Line or Width Limit Feature Not Used, Any Memory Areas Can Be Overwritten 	
	 Advisory 2.1.62, HDVPSS: Discrete Sync Interlaced Output Mode: Vertical Sync Output For Odd Fields May Not Correctly Detect Video Signal 	
	 Advisory 2.1.83, HDVPSS: VIP Single-Channel Capture Using Tiled Output Can Lead To VIP Lockup if Connect/Disconnect Events Occur 	
	 Advisory 2.1.66, PCI Express (PCIe): PCIe Boot Fails When Connected to Some PCs 	
	 Advisory 2.1.88, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth 	
	Advisory 2.1.70, USB: A USB Device that Responds to a Spurious Invalid Short Packet may Lock up the Bus	
	Advisory 2.1.71, ROMCODE: PCIe Boot is Unstable	
	 Advisory 2.1.72, ROMCODE: ROM Code Does Not Support Booting from eMMC Devices of Size 4GB or Mon Advisory 2.1.78, UABT, Suba Association of the SISO Tensorial DMA Research UABT, DMA TX 	
	 Advisory 2.1.76, UART: Extra Assertion of the FIFO Transmit DMA Request, UARTi_DMA_TX Advisory 2.1.76, EDMA_TCO and TCA Panel Assertion Always Use Physical Advances 	
	 Advisory 2.1.79, EDMA: TC0 and TC1 Read Accesses Always Use Physical Address Advisory 2.1.99, Bowe Segmenting CVDD accesses Always Use Physical Address 	
	 Advisory 2.1.80, Power Sequencing: CVDD versus CVDD_* Advisory 2.1.81, Power Sequencing: 3.3V DVDD* versus VDDA 1P8 	
	 Advisory 2.1.82, Power Sequencing: DVDD_DDR[x] versus 3.3V DVDD* Supplies Advisory 2.1.84, MLB: Potential for Misaligned Data in Multi-Frame per Sub-buffer Mode 	
	 Advisory 2.1.84, MLB. Potential for Misaligned Data in Multi-Prame per Sub-burier Mode Advisory 2.1.85, EMAC and Switch Subsystem: Reset Isolation Feature is Not Supported 	
	 Advisory 2.1.85, EmAC and Switch Subsystem. Reset isonation readine is Not Supported Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power- On Hours May Occur if the Input Receiver is Disabled 	
	 Advisory 2.1.88, Control Module, Pin Configuration (PINCNTLx): ROM Modifies Bit 19 	

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AM387x Sitara™ ARM® Microprocessors (MPUs) Silicon Revisions 3.0, 2.1

Silicon Errata

Literature Number: SPRZ345C September 2011-Revised March 2013

TEXAS INSTRUMENTS

This silicon errata revision history highlights the technical changes made to the SPRZ345A revision to make it an SPRZ345B revision, as well as the technical changes made to the SPRZ345B revision to make it an SPRZ345C revision.

Scope: Applicable updates relating to the AM387x devices have been incorporated.

AM387x Revision History

0.5.5		
SEE	ADDITIONS/MODIFICATIONS/DELETIONS	
Revision C (Silicor	n Revision 3.0) Changes below:	
Global	Added Silicon Revision 3.0 device-specific data	
Section 1.2	Package Symbolization and Revision Identification:	
	 Updated/Changed "Figure 1 shows" paragraph 	
Figure 1	Example, Device Revision Codes:	
	 Updated figure to show an example of silicon revision 3.0 ("C") 	
Table 1	AM387x Device Revision Codes:	
	 Added Silicon Revision 3.0 ("C") device-specific data 	
Section 2	Silicon Revision 3.0 Usage Notes and Known Design Exceptions to Functional Specifications:	
	Added new section	
Section 2.1	Usage Notes for Silicon Revision 3.0:	
	Added new section	
	Moved the following 2.1 Usage Notes to this new section:	
	Section 2.1.1, DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit Section 2.1.2, Serve Bills Only Suggest First N2 Best Divides:	
	 Section 2.1.2, Some PLLs Only Support Even M2 Post Dividers Section 2.1.3, DDR2 and DDR3 Requires Software Leveling 	
Section 2.2	Silicon Revision 3.0 Known Design Exceptions to Functional Specifications:	
Section 2.2	Added new section	
	Moved all other 2.1 Advisories to this section except for these:	
	· ·	
	 Advisory 2.1.27, SATA: Unable to Operate Both SATA and VOUT0 Without SATA Locking Up 	
	 Advisory 2.1.28, SATA: Link Establishment Fails With SATA GEN3 Capable Targets 	
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After 	
	HDVPSS Reset or VIP Client Abort Causes Lockup	
	 Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring 	
	Advisory 2.1.68. DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors	5
	for DDR Bandwidth	
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction 	
	in Power-On Hours May Occur if the Input Receiver is Disabled	
Section 3.1	Usage Notes for Silicon Revision 2.1:	
Section 5.1	Updated/Changed "Silicon revision 2.1 applicable usage notes" paragraph	
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:	
	 Updated/Changed "This is a list of the device revision 2.1 known" paragraph 	
	 Added Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performin 	ng
	Single-Channel Capture, Section Tiled Data to DDD and Connect/Discovered Function Convertion	
	Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring	
RZ345C-Septembe	er 2011-Revised March 2013 Revision Histor	y

AM387x Revision History

SEE	SEE ADDITIONS/MODIFICATIONS/DELETIONS	
Revision B (Silic	on Revision 2.1) Changes below:	
Global	Updated/Changed "Digital Media Processors" to "Video Processors"	
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:	
	Updated/Changed the Data Manual Doc Titles	
	Added the following Advisories to this section:	
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup 	
	 Advisory 2.1.54, VPDMA Line Limit Feature: Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields in Memory 	
	 Advisory 2.1.55, HPVPSS VIP Inline Color Space Converter (CSC): In Interlaced Embedded or Discrete Sync Mode, Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields In Memory 	
	 Advisory 2.1.58, HDVPSS: HDVPSS VIP Reset Sequence is Occasionally Unsuccessful if VPDMA is Writing Output Descriptors for VIP Captured Data 	
	 Advisory 2.1.60, HDVPSS: Occasionally, During Connect/Disconnect and When Line or Width Limit Feature Not Used, Any Memory Areas Can Be Overwritten 	
	 Advisory 2.1.62, HDVPSS: Discrete Sync Interlaced Output Mode: Vertical Sync Output For Odd Fields May Not Correctly Detect Video Signal 	
	 Advisory 2.1.63, HDVPSS: VIP Single-Channel Capture Using Tiled Output Can Lead To VIP Lockup if Connect/Disconnect Events Occur 	
	 Advisory 2.1.88, PCI Express (PCIe): PCIe Boot Fails When Connected to Some PCs 	
	 Advisory 2.1.68, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth 	
	· Advisory 2.1.70, USB: A USB Device that Responds to a Spurious Invalid Short Packet may Lock up the Bus	
	Advisory 2.1.71, ROMCODE: PCIe Boot is Unstable	
	 Advisory 2.1.72, ROMCODE: ROM Code Daes Not Support Booting from eMMC Devices of Size 4GB or More 	
	 Advisory 2.1.76, UART: Extra Assertion of the FIFO Transmit DMA Request, UARTi_DMA_TX 	
	 Advisory 2.1.79, EDMA: TC0 and TC1 Read Accesses Always Use Physical Address 	
	 Advisory 2.1.80, Power Sequencing: CVDD versus CVDD_ARM 	
	 Advisory 2.1.81, Power Sequencing: 3.3V DVDD* versus VDDA_1P8 	
	 Advisory 2.1.82, Power Sequencing: DVDD_DDR[x] versus 3.3V DVDD* Supplies 	
	 Advisory 2.1.85, EMAC and Switch Subsystem: Reset Isolation Feature is Not Supported 	
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power- On Hours May Occur if the Input Receiver is Disabled 	
	Advisory 2.1.88, Control Module, Pin Configuration (PINCNTLx): ROM Modifies Bit 19	
OTE: Page numb	ers for previous revisions may differ from page numbers in the current version.	



This silicon errata revision history highlights the technical changes made to the SPRZ361A revision to make it an SPRZ361B revision, as well as the technical changes made to the SPRZ361B revision to make it an SPRZ361C revision.

Scope: Applicable updates relating to the TMS320DM814x devices have been incorporated.

DM814x	Revision	History
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SEE	ADDITIONS/MODIFICATIONS/DELETIONS
evision C (Silico	n Revision 3.0) Changes below:
Global	Added Silicon Revision 3.0 device-specific data
Section 1.2	Package Symbolization and Revision Identification:
	Updated/Changed "Figure 1 shows" paragraph
Figure 1	Example, Device Revision Codes:
	 Updated figure to show an example of silicon revision 3.0 ("C" or "S")
Table 1	TMS320DM814x Device Revision Codes:
	 Added Silicon Revision 3.0 ("C") device-specific data
Section 2	Silicon Revision 3.0 Usage Notes and Known Design Exceptions to Functional Specifications:
	Added new section
Section 2.1	Usage Notes for Silicon Revision 3.0:
	Added new section
	Moved the following 2.1 Usage Notes to this new section:
	Section 2.1.1, DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit Section 2.1.2, Spran PL a Only Surged Fund M2 Rest Divider:
	Section 2.1.2, Some PLLs Only Support Even M2 Post Dividers Section 2.1.3, DDR2 and DDR3 Requires Software Leveling
Section 2.2	Silicon Revision 3.0 Known Design Exceptions to Functional Specifications:
Section 2.2	Added new section
	Moved all other 2.1 Advisories to this section except for these:
	•
	 Advisory 2.1.27, SATA: Unable to Operate Both SATA and VOUT0 Without SATA Locking Up
	 Advisory 2.1.28, SATA: Link Establishment Fails With SATA GEN3 Capable Targets
	 Advisory 2.1.51,HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lookup
	 Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring
	 Advisory 2.1.68, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power-On Hours May Occur if the Input Receiver is Disabled
Section 3.1	Usage Notes for Silicon Revision 2.1:
	 Updated/Changed "Silicon revision 2.1 applicable usage notes" paragraph
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:
	 Updated/Changed "This is a list of the device revision 2.1 known" paragraph
	 Added Advisory 2.1.59, HDVPSS: Occasionally, Chip Lockup Occurs When HDVPSS VIP is Performing Single Changed Casters
	Single-Channel Capture, Sending Tiled Data to DDR and Connect/Disconnect Events are Occurring
	er 2011-Revised March 2013 Revision History
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	DM814x Revision History (continued)
SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Revision B (Silic	on Revision 2.1) Changes below:
Global	Updated/Changed "DEMMU" to "System MMU"
	Updated/Changed "Digital Media Processors" to "Video Processors"
Section 3.2	Silicon Revision 2.1 Known Design Exceptions to Functional Specifications:
	Updated/Changed the Data Manual Doc Titles
	Advisory 2.1.25, System DEMMU May Hang When Used in Table-Walk Mode:
	 Updated/Changed the System MMU Entries (Entry 1 through Entry 7) code in the System MMU Lockdown Example.
	Added the following Advisories to this section:
	 Advisory 2.1.51, HDVPSS: VIP Capture of One-Line Frame to VIP LO Port Immediately After HDVPSS Reset or VIP Client Abort Causes Lockup
	 Advisory 2.1.54, VPDMA Line Limit Feature: Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields in Memory
	 Advisory 2.1.55, HPVPSS VIP Inline Color Space Converter (CSC): In Interlaced Embedded or Discrete Sync Mode, Descriptor Reports All Fields as Even, but Captures 30 Even and 30 Odd Fields In Memory
	 Advisory 2.1.58, HDVPSS: HDVPSS VIP Reset Sequence is Occasionally Unsuccessful if VPDMA is Writing Output Descriptors for VIP Captured Data
	 Advisory 2.1.60, HDVPSS: Occasionally, During Connect/Disconnect and When Line or Width Limit Feature Not Used, Any Memory Areas Can Be Overwritten
	 Advisory 2.1.62, HDVPSS: Discrete Sync Interlaced Output Mode: Vertical Sync Output For Odd Fields May Not Correctly Detect Video Signal
	 Advisory 2.1.63, HDVPSS: VIP Single-Channel Capture Using Tiled Output Can Lead To VIP Lockup if Connect/Disconnect Events Occur
	 Advisory 2.1.66, PCI Express (PCIe): PCIe Boot Fails When Connected to Some PCs
	 Advisory 2.1.68, DDR DMM: Continuous Writes From Cortex-A8 Occasionally Starve Other Requestors for DDR Bandwidth
	 Advisory 2.1.70, USB: A USB Device that Responds to a Spurious Invalid Short Packet may Lock up the Bus Advisory 2.1.71, ROMCODE: PCIe Boot is Unstable
	 Advisory 2.1.72, ROMCODE: ROM Code Does Not Support Booting from eMMC Devices of Size 4GB or More Advisory 2.1.76, UART: Extra Assertion of the FIFO Transmit DMA Request, UARTi DMA TX
	 Advisory 2.1.79, EDMA: TC0 and TC1 Read Accesses Always Use Physical Address
	 Advisory 2.1.80, Power Sequencing: CVDD versus CVDD *
	 Advisory 2.1.81, Power Sequencing: 3.3V DVDD* versus VDDA_1P8
	 Advisory 2.1.82, Power Sequencing: DVDD_DDR[x] versus 3.3V DVDD* Supplies
	 Advisory 2.1.85, EMAC and Switch Subsystem: Reset Isolation Feature is Not Supported
	 Advisory 2.1.87, Control Module, Pin Configuration (PINCNTLx), 3.3 V Mode Operation: Reduction in Power- On Hours May Occur if the Input Receiver is Disabled
	 Advisory 2.1.88, Control Module, Pin Configuration (PINCNTLx): ROM Modifies Bit 19
)TE: Page numb	ers for previous revisions may differ from page numbers in the current version.

The datasheet number will be changing.

Device Family	Change	Change To:
	From:	
DM814x	SPRZ343A	SPRZ343C
DM812x	SPRZ385	SPRZ385B
DRA64x/DRA65x	SPRZ346	SPRZ346B
AM387x	SPRZ345A	SPRZ345C
DM814xSEC	SPRZ361A	SPRZ361C

Reason for Change:

To more accurately reflect device characteristics

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Electrical specification performance changes as indicated above.

Changes to product identification resulting from this PCN:

None

None			
Product Affected:			
AM3871CCYE100	DRA655AVWBICYERQ1	TMS320DM8148CCYE0	TMX320DM8148CYE
AM3871CCYE80	DRA657CICYERQ1	TMS320DM8148CCYE1	TMX320DRA6XXCYE
AM3874BCYE100	TDA1MEDBCYEQ7Q1	TMS320DM8148CCYE2	XAM3874BCYE
AM3874BCYE80	TDA1MSACCYEQ4Q1	TMS320DM8148CCYE2F	XDRA62XAZKK
AM3874CCYE100	TDA1MSVBCYEQ5Q1	TMS320DM8148CCYEA0	XDRA62XHSAZKK
AM3874CCYE80	TMS320DM8127BCYE3	TMS320DM8148SCYE0	XDRA65XBCYEP
AM3874CCYEA80	TMS320DM8127BCYED3	TMS320DM8148SCYE1	XDRA6XXBCYE
DM8148CR2CYE2	TMS320DM8147BCYE0	TMS320DM8148SCYE2	XDRA6XXBCYEF
DRA631AIZKKQ1	TMS320DM8147BCYE1	TMS320DM8148SCYEA0	XDRA6XXCCYE
DRA633AIZKKQ1	TMS320DM8147BCYE2	TMX320C6A8148BCYE	XTDA1MEVAASQX
DRA643CICYEQ1	TMS320DM8147SCYE1	TMX320DM8147BCYE0	XTDA1MEVCYEQX
DRA644BICYEQ1	TMS320DM8147SCYE2	TMX320DM8147BCYE1	XTDA1MXXBCYEQX
DRA646BICYEQ1	TMS320DM8148BCYE0	TMX320DM8147BCYE2	XTDA1MXXCCYEQX
DRA647CICYEQ1	TMS320DM8148BCYE1	TMX320DM8148BCYE	
DRA648CICYEQ1	TMS320DM8148BCYE2	TMX320DM8148CCYE2	

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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