4.5-V To 18-V Input Voltage, 3.5-A/3.5-A Dual Synchronous Step-Down Converter With I²C Controlled VID

FEATURES

- **4.5-V to 18-V Wide Input Voltage Range**
- **I²C Controlled 7-Bits VID Programmable Output Voltage from 0.68 V to 1.95 V with 10-mV Steps for Each Buck; Output Voltage can also be Set by Resistor Divider**
- **Programmable Slew-Rate Control for Output-Voltage Transition**
- **Up to 3.5-A Maximum Continuous Output Current in Buck 1 and Buck 2**
- **Buck 1 and Buck 2 can be Paralleled to Deliver up to 7-A Current**
- **I²C Compatible Interface With Standard Mode (100 kHz) and Fast Mode (400 kHz)**
- **I²C Read Back Power Good Status and Die Temperature Warning**
- **Pulse-Skipping Mode to Achieve High Efficiency in Light Loads**
- **Adjustable Switching Frequency 200 kHz to 1.6 MHz Set by External Resistor**
- **Dedicated Enable and Soft-Start for Each Buck**
- **Peak Current-Mode Control With Simple Compensation Circuit**
- **Cycle-by-Cycle Overcurrent Protection**
- **180° Out-of-Phase Operation to Reduce Input Filter and Power Supply Conduced Noise**
- **Overtemperature Protection**
- **Available in 32-Pin Thermally Enhanced HTSSOP (DAP) Package**

APPLICATIONS

- **DTV**
- **TCON**
- **BDVD**
- **Set Top Boxes**
- **Tablet PC**

DESCRIPTION

The TPS563900 device is a monolithic dual-synchronous buck converter with a wide 4.5-V to 18-V operating input-voltage range that can operate in 5-, 9-, 12-, or 15-V bus voltages and battery chemistries. Constant-frequency peak-current mode control simplifies the loop compensation and provides fast transient response.

External feedback resistors can be used to set the initial start-up voltage for each buck converter in the TPS563900 device. The feedback voltage reference for this start-up option is 0.6 V. When the voltage-identification (VID) DAC is updated through the I²C, the buck converter switches the feedback resistors from external to internal feedback resistors. The output voltage in each buck is programmable from 0.68 V to 1.95 V with 10-mV steps by I²C-controlled 7-bit VID.

Each buck converter in the TPS563900 device can also be I²C controlled for enabling and disabling the output voltage, reading the output voltage, setting the pulse skipping mode, and reading the power good status and the warning of die temperature.

The TPS563900 device features a dedicated enable pin when the I²C interface is not used. An independent soft-start pin provides flexibility in power-up programmability. Cycle-by-cycle overcurrent protection and hiccup-mode operation limit MOSFET power dissipation in short circuit or over-loading fault conditions. Low-side reverse overcurrent protection also prevents excessive sinking current from damaging the converter.

The TPS563900 device also features a light-load pulse-skipping mode (PSM) that can be controlled by the I²C or MODE pin configuration. The PSM mode allows a power loss reduction on the input power supplied to the system to achieve high efficiency at light loading.

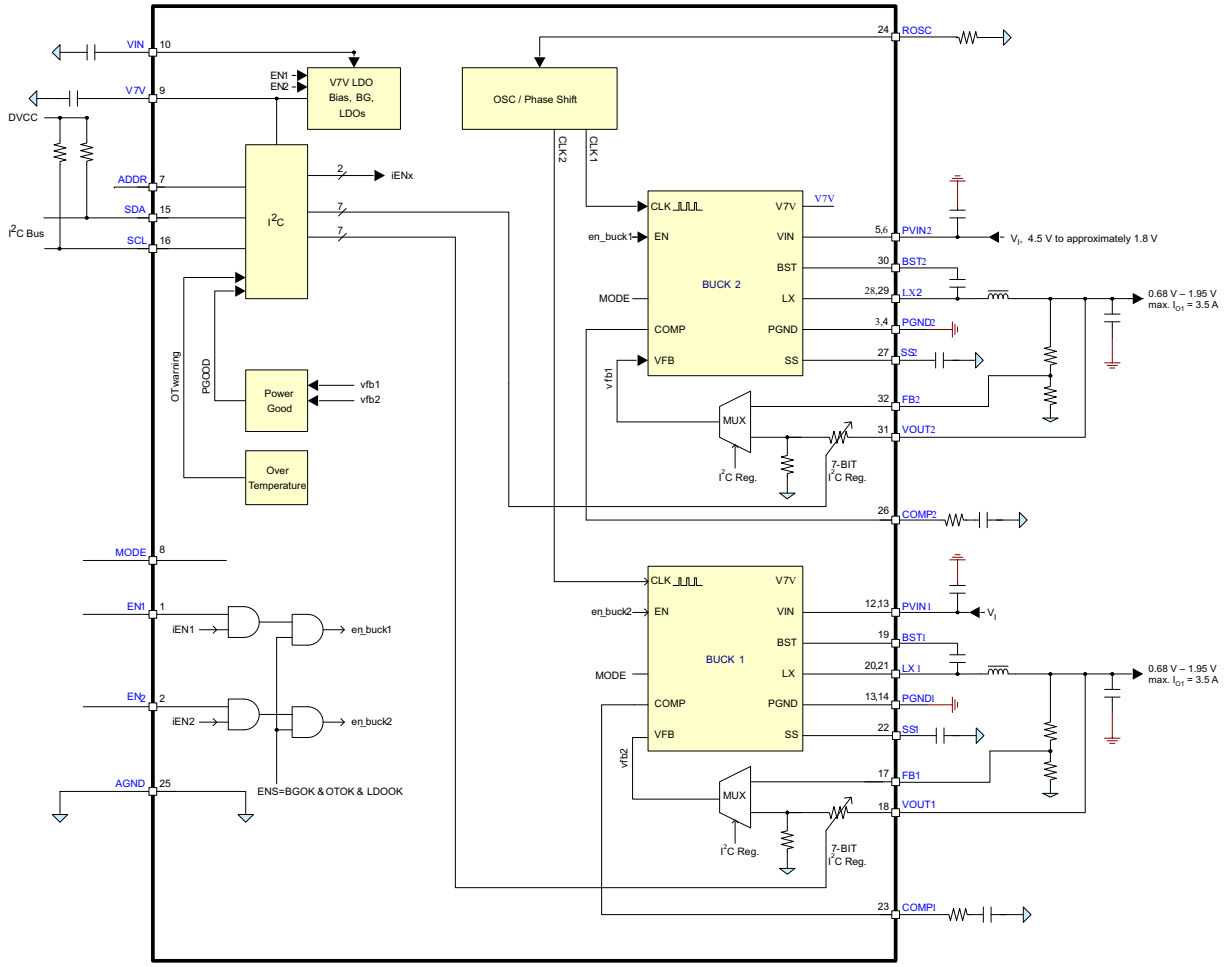
The TPS563900 device is available in a 32-lead thermally-enhanced HTSSOP (DAP) package.

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

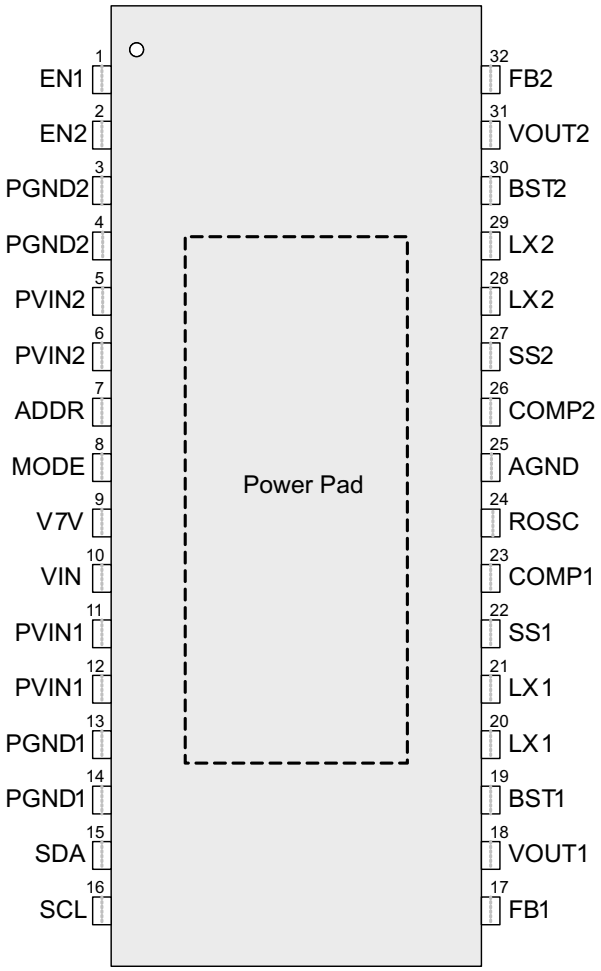
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL CONFIGURATION

DAP PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

TERMINAL FUNCTIONS

NAME	NO. (HTSSOP)	DESCRIPTION
EN1, EN2	1, 2	Enable pin. Adjust the input under-voltage lockout with two resistors.
PGND2	3, 4	Power ground of Buck 2, place the ground pin of this input capacitor as close as possible to this pin.
PVIN2	5, 6	Power input. Input power supply to the power switches of the power converter 2.
ADDR	7	I^2C address configuration pin. Connect this pin to low, high, or leave it open to select different I^2C slave address.
MODE	8	Operation-mode control pin. Connect this pin to ground to choose forced PWM mode; leave the pin open for pulse skipping mode (PSM) operation at light load condition.
V7V	9	Internal low-drop linear regulator (LDO) output to power internal driver and control circuits. Decouple this pin to power ground with a minimum 1-μF ceramic capacitor. The output regulates to 6.3 V (typical) for optimal conduction on-resistances of the internal power MOSFETs. In PCB design, the power ground and analog ground must have one-point common connection at the negative terminal of the V7V bypass capacitor. If VIN is lower than 6.3 V, V7V is slightly lower than VIN.
VIN	10	Power supply of the internal LDO and controllers
PVIN1	11, 12	Power input. Input power supply to the power switches of the power converter 1.
PGND1	13, 14	Power ground of Buck 1, place the ground pin of the input capacitor as close as possible to this pin.
SDA	15	I^2C interface data pin
SCL	16	I^2C interface clock pin
FB1	17	Feedback sensing pin for the external feedback resistors in Buck 1. Before I^2C-controlled VID selection is enabled, an external resistor divider connected to this pin sets the initial output voltage.
VOUT1	18	Buck 1 output voltage sensing pin; When I^2C controlled VID selection is enabled, output voltage can be programmed from 0.68 V to 1.95 V with 10-mV steps.
BST1	19	Supply input for the high-side NFET gate drive circuit of Buck 1. Connect a ceramic capacitor between the BST1 and LX1 pins.
LX1	20, 21	Switching node of Buck 1
SS1	22, 27	Soft start and voltage tracking in Buck 1. An external capacitor connected to this pin sets the internal voltage reference rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
COMP1	23	Error amplifier output and loop compensation pin for Buck 1. Connect frequency compensation to this pin.
ROSC	24	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency. When connected to an external clock, the internal oscillator synchronizes to the external clock.
AGND	25	Analog ground of the converter. Connect sensitive (such as SSx and FBx) returns to AGND at a single point.
COMP2	26	Error amplifier output and loop compensation pin for Buck 2. Connect frequency compensation to this pin.
SS2	27	Soft-start and voltage tracking in Buck 2. An external capacitor connected to this pin sets the internal voltage reference rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and power sequencing.
LX2	28, 29	Switching nodes
BST2	30	Supply input for high-side NFET gate drive circuit of Buck 2. Connect a ceramic capacitor between BST2 and LX2 pins.
VOUT2	31	Buck 2 output voltage sensing pin. When I^2C-controlled VID selection is enabled, the output voltage can be programmed from 0.68 V to 1.95 V with 10-mV steps.
FB2	32	Feedback sensing pin for the external feedback resistors in Buck 2. Before I^2C-controlled VID selection is enabled, an external resistor divider connected to this pin sets the initial output voltage.
Exposed Thermal Pad	33	Exposed thermal pad of the package. Connect to the power ground. There is no electric signal down bonded to the thermal pad inside the IC package. TI highly recommends to always solder this thermal pad to PCB board, and have as many vias as possible on the PCB to enhance power dissipation.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
	Voltage range at VIN, PVIN1,PVIN2	–0.3	20	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns)	–1	20	V
	Voltage at BST1, BST2, referenced to LX1, LX2 pin	–0.3	7	V
	Voltage at V7V, EN1, EN2, VOUT1, VOUT2, MODE	–0.3	7	V
	Voltage at SS1, SS2, FB1, FB2, COMP1, COMP2	–0.3	3	V
	Voltage at SDA, SCL, ADDR, EN1, EN2, ROSC	–0.3	7	V
	Voltage at AGND, PGND1, PGND2	–0.3	0.3	V
T_J	Operating virtual junction temperature range	–40	125	°C
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		TPS563900 DAP 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	35	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	17.7	
θ_{JB}	Junction-to-board thermal resistance(3)	19	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(5)	18.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	1.3	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_A	Ambient temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

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ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_I = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_I	Input voltage range	VIN1 and VIN2	4.5		18	V
IDD_{SD}	Shutdown supply current	EN1 = EN2 = low		10		µA
IDD_{Q_NSW}	Switching quiescent current with no load at DCDC output	EN1 = EN2 = 3.3 V Without bucks switching		1.2		mA
IDD_{Q_SW}	Switching quiescent current with no load at DCDC output, Buck switching	EN1 = EN2 = 3.3 V With bucks switching		10		mA
UVLO	V_I under voltage lockout	Rising V_I		4.25	4.5	V
		Falling V_I	3.5	3.75		
		Hysteresis		0.5		
V_{7V}	6.3 V LDO	V7V load current = 0 A, V_I = 12 V	6.1	6.3	6.5	V
I_{OCP_V7V}	Current-limit of V7V LDO			200		mA
ENABLE						
V_{ENR}	Enable threshold			1.21	1.26	V
V_{ENF}	Enable threshold		1.1	1.17		V
I_{ENR}	Enable Input current	EN = 1 V		3		µA
I_{ENF}	Enable hysteresis current	EN = 1.5 V		3		µA
OSCILLATOR						
f_{SW}	Switching frequency		200		1600	kHz
		ROSC = 100 kΩ (1%)	340	400	460	
T_{SYNC_w}	Clock sync minimum pulse width				20	ns
V_{SYNC_HI}	Clock sync high threshold				2	V
V_{SYNC_LO}	Clock sync low threshold		0.8			V
V_{SYNC_D}	Clock falling edge to LX rising edge delay			66		ns
f_{SYNC}	Clock sync frequency range		200		1600	kHz
BUCK 1, BUCK 2 CONVERTERS						
$V_{ref(min)}$	Voltage reference	0 A < $I_{O1,2}$ < 3.5 A	0.594	0.6	0.606	V
$V_{O1,2}$	Output voltage step size (VID 0x00 – 0x7F)		8	10	12	mV
$\Delta V_{O(\Delta VI)}$	Line regulation—DC	I_O = 2 A		0.5		%/V
$\Delta V_{O(\Delta IL)}$	Load regulation—DC	I_O = (10 to 90%) x I_{O_max}		0.5		%/A
g_{m_EA3}	Error amplifier trans-conductance	–2 µA < I_{COMP} < 2 µA		1350		µS
g_{m_SRC3}	COMP voltage to inductor current G_m	I_{LX} = 0.5 A		10		A/V
I_{SSx}	Soft-start pin charging current	SS1, SS2		6		µA
I_{L1}	Buck 1 peak inductor current-limit			4.5		A
I_{L2}	Buck 2 peak inductor current-limit			4.5		A
I_{LLSx}	Low-side sinking current-limit			–2.6		A
$R_{DS(on)x\_HS}$	On-resistance of high-side FET	V7V = 6.3 V		90		mΩ
$R_{DS(on)x\_LS}$	On-resistance of low-side FET	V_I = 12 V		65		mΩ
$t_{on(min)}$	Minimum on time			94	145	ns
V_{bootUV}	Boot-LX UVLO			2.1	3	V
$t_{hiccupwait}$	Hiccup wait time			512		cycles
t_{hiccup_re}	Hiccup time before re-start			16 384		cycles

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

T_J = 25°C, V_I = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C READ BACK FAULT STATUS						
V_{PGOOD}	PGOOD trip levels	Feedback lower voltage rising (with respect to 0.6 V)		94.0		%
		Feedback lower voltage falling (with respect to 0.6 V)		92.5		
		Feedback upper voltage rising (with respect to 0.6 V)		107.5		
		Feedback upper voltage falling (with respect to 0.6 V)		105.5		
T_{warn}	Temperature warning threshold			125		°C
THERMAL SHUTDOWN						
T_{TRIP}	Thermal protection trip point	Rising temperature		160		°C
T_{hys}	Thermal protection hysteresis			20		°C
I²C INTERFACE						
V_{IH} SDA, SCL	Input high voltage				1.3	V
V_{IL} SDA, SCL	Input low voltage		0.4			V
I_I	Input current	SDA, SCL, V_I = 0.4 V to 4.5 V	–10		10	µA
V_{OL} SDA	SDA output low voltage	SDA open drain, I_{OL} = 4 mA			0.4	V
f_{max}	Maximum SCL clock frequency		400			kHz
t_{BUF}	Bus-free time between a STOP and START condition		1.3			µs
t_{h_STA}	Hold time (Repeated) START condition		0.6			µs
t_{su_STO}	Setup time for STOP condition		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{su_STA}	Setup time for a repeated START condition		0.6			µs
t_{SU_DAT}	Data setup time		0.1			µs
t_{h_DAT}	Data hold time		0		0.9	µs
t_{rCL}	Rise time of SCL signal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{rCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{fCL}	Fall time of SCL sgnal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{rDA}	Rise time of SDA signal	Capacitance of one bus line (pF)	$20 + 0.1C_B$		300	ns
t_{fDA}	Fall time of SDA signal	Capacitance of one bus line(pF)	$20 + 0.1C_B$		300	ns
C_B	Capacitance of one bus line (SCL and SDA)				400	pF

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

T_A = 25°C, V_I = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

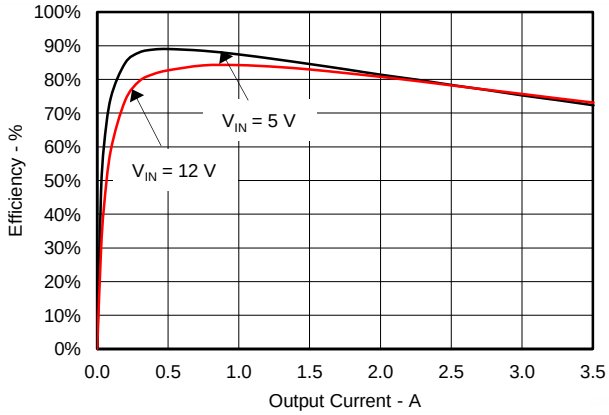


Figure 1. 1-V Efficiency

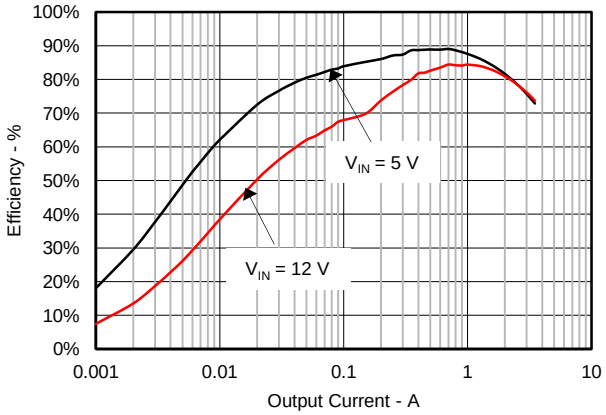


Figure 2. 1-V Efficiency, Eco-mode™

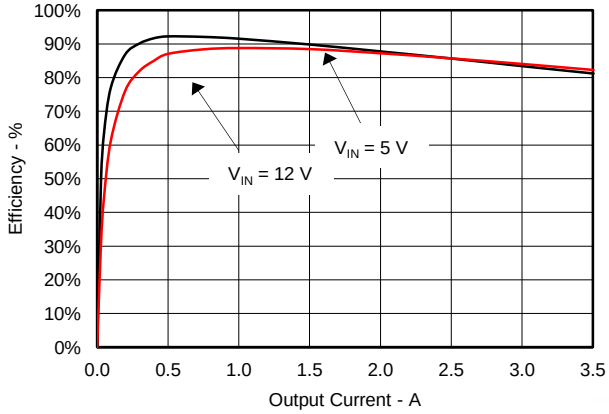


Figure 3. 1.8-V Efficiency

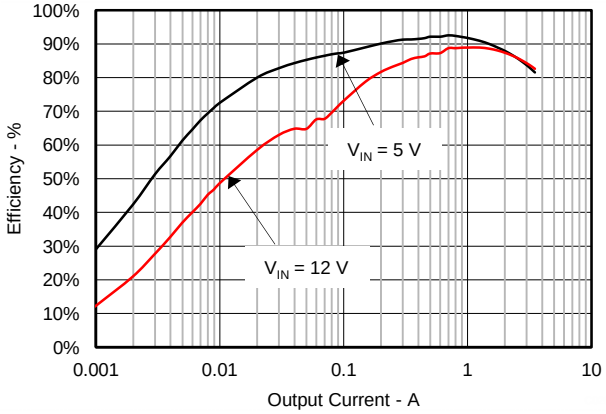


Figure 4. 1.8-V Efficiency, Eco-mode

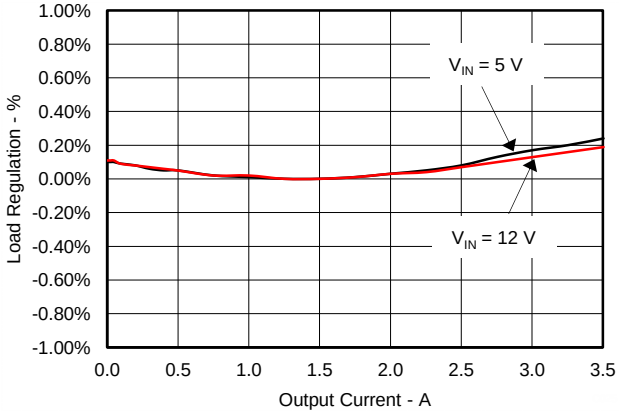


Figure 5. 1-V Load Regulation

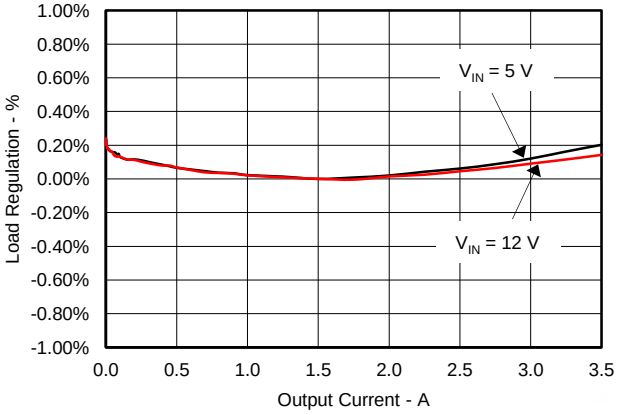


Figure 6. 1-V Load Regulation, Eco-mode

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_I = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

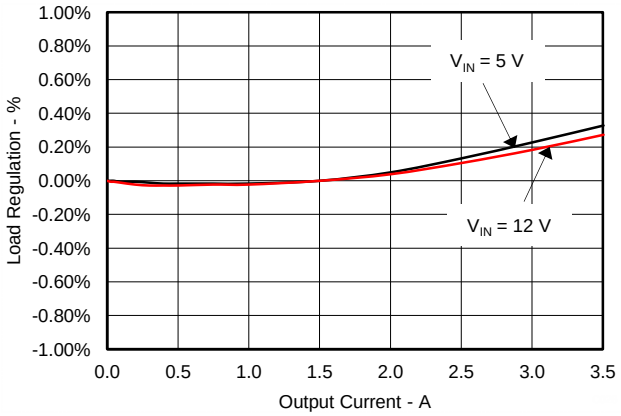


Figure 7. 1.8-V Load Regulation

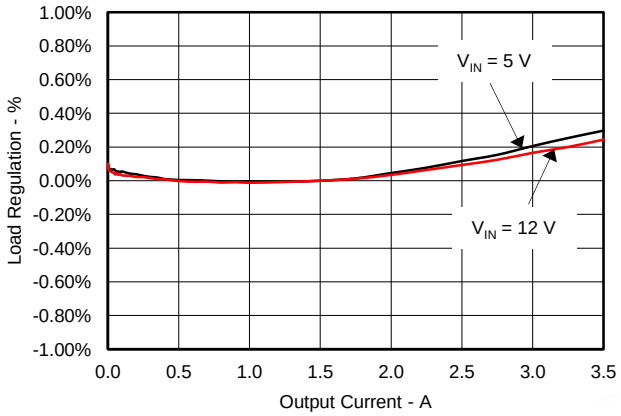


Figure 8. 1.8-V Load Regulation, Eco-mode

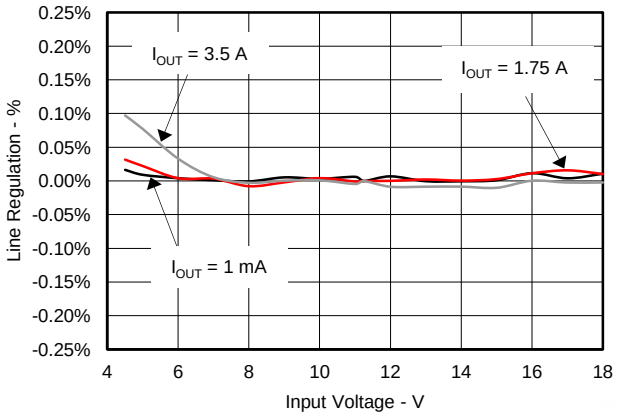


Figure 9. Line Regulation, $V_{OUT}1$ = 1.0 V, Eco-mode = OFF

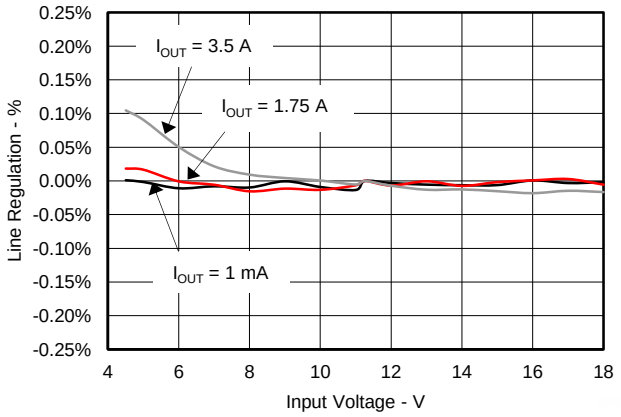
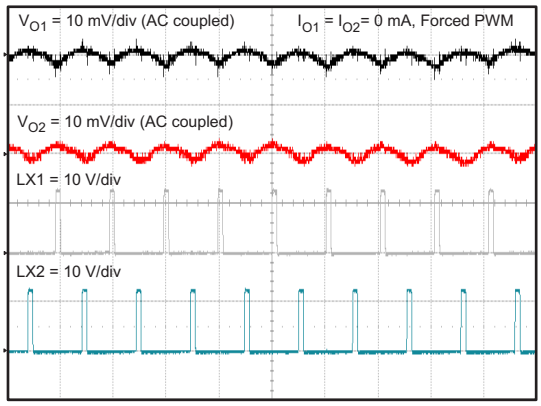
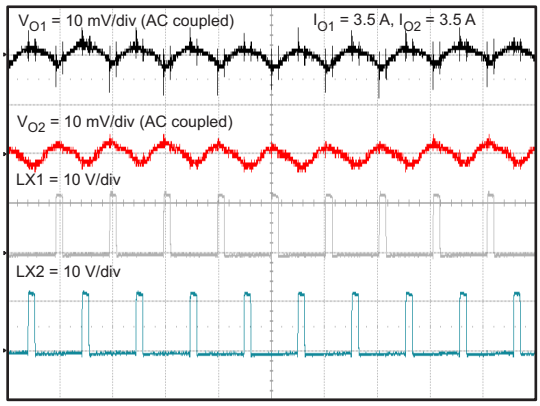


Figure 10. Line Regulation, $V_{OUT}2$ = 1.0 V, Eco-mode = OFF



Time = 2 µs/div

Figure 11. Output Ripple at 0 A, Forced PWM



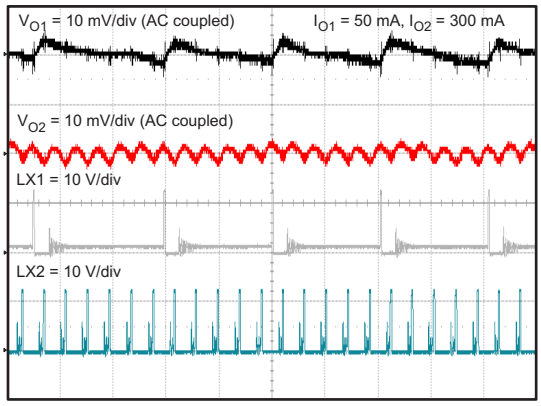
Time = 2 µs/div

Figure 12. Output Ripple at 3.5 A, Forced PWM

PRODUCT PREVIEW

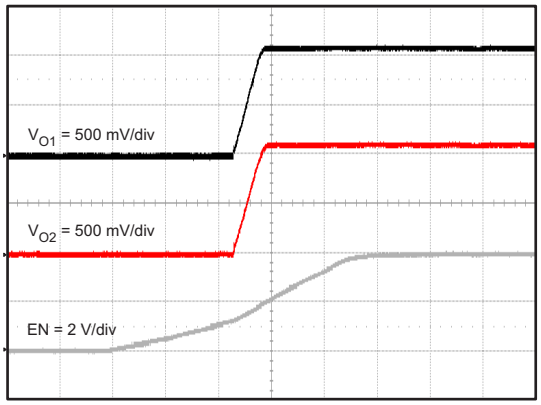
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_I = 12 V, f_{SW} = 500 kHz (unless otherwise noted)



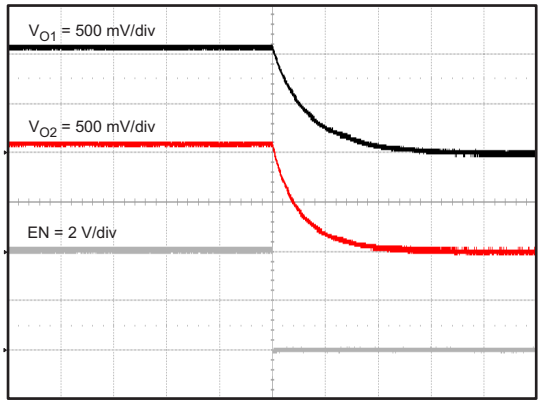
Time = 5 µs/div

Figure 13. Output Ripple, Buck1 at 0.05 A, Buck 2 at 0.3 A Auto PSM-PWM Mode



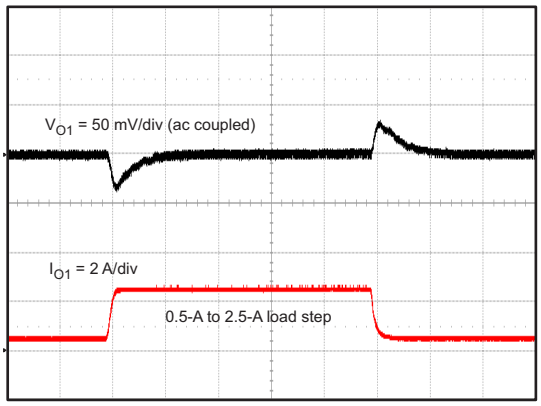
Time = 2 ms/div

Figure 14. Startup With Enable



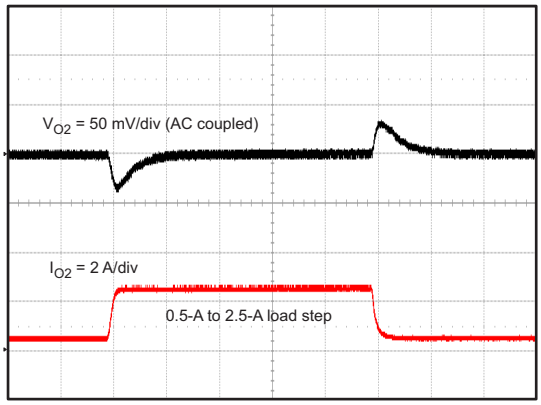
Time = 1 ms/div

Figure 15. Shutdown With Enable



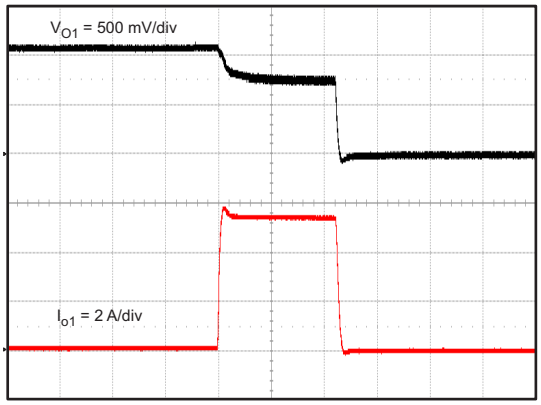
Time = 100 µs/div

Figure 16. Load Transient, Buck 1 (0.5 A to 2.5 A)



Time = 100 µs/div

Figure 17. Load Transient, Buck 2 (0.5 A to 2.5 A)



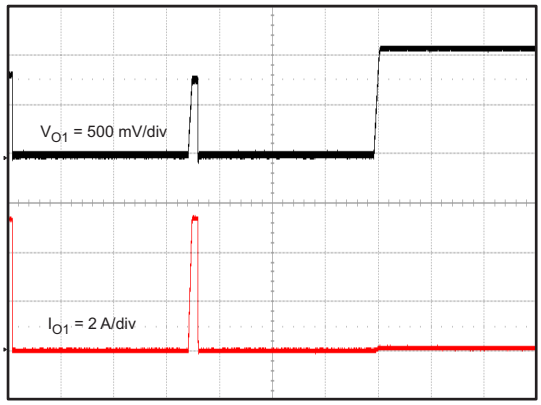
Time = 500 µs/div

Figure 18. Overcurrent Protection, Buck 1

PRODUCT PREVIEW

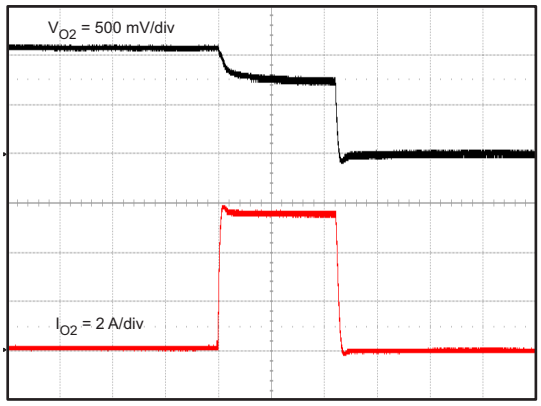
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_I = 12 V, f_{SW} = 500 kHz (unless otherwise noted)



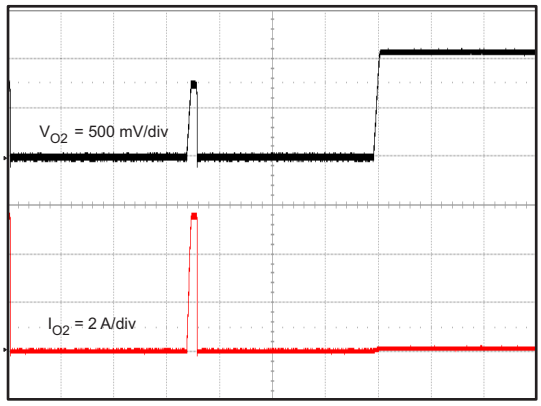
Time = 10 ms/div

Figure 19. Hiccup Recover, Buck 1



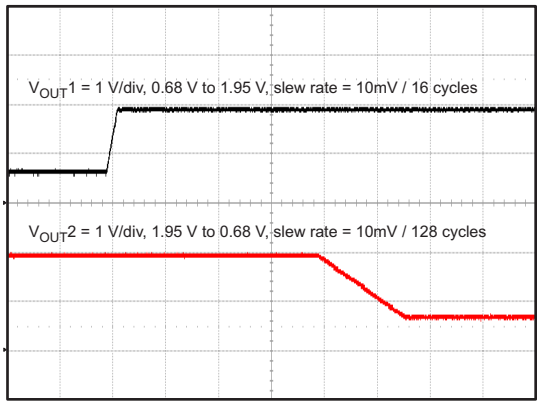
Time = 500 µs/div

Figure 20. Overcurrent Protection, Buck 2



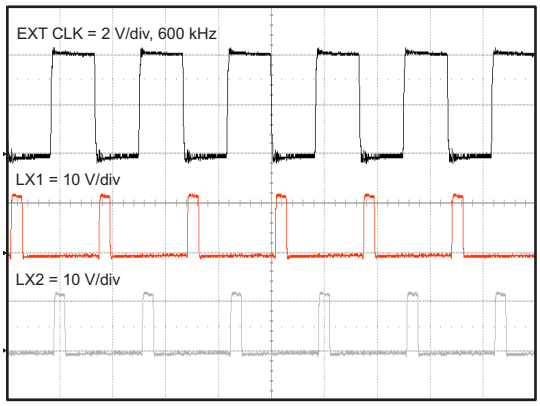
Time = 10 ms/div

Figure 21. Hiccup Recover, Buck 2



Time = 20 ms/div

Figure 22. Voltage Change With I^2C Control



Time = 1 µs/div

Figure 23. Synchronization at 600 kHz

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OVERVIEW

The TPS563900 device is a dual 3.5-A/3.5-A output current, synchronous step-down (buck) converter with integrated N-channel MOSFETs. A wide 4.5-V to 18-V input supply range to buck encompasses most intermediate bus voltages operating off 9-V, 12-V, or 15-V power bus.

The TPS563900 device is equipped with an I^2C-compatible bus for sophisticated control and communication with SoC. With an I^2C interface, SoC can enable or disable the power converters, set the output voltage, and read status registers. The buck regulator has external feedback resistors that can be used for setting the initial start-up voltage. The feedback voltage reference for this start-up option is 0.6 V. When the voltage identification VID DAC is updated through the I^2C, the output voltage of each channel can be independently programmed with 7-bit VID from 0.68 V to 1.95 V in 10-mV steps. The output-voltage transitions begin when the I^2C interface receives the command for the GO bit in the command registers. In light loading condition, the I^2C can control or select low-pulse skipping mode with MODE-pin configuration.

The TPS563900 device implements a constant frequency, peak current-mode control which simplifies external frequency compensation. The wide switching frequency of 200 kHz to 1600 kHz allows for efficiency and size optimization when selecting the output filter components. An external resistor to ground on the ROSC pin can adjust the switching frequency. The TPS563900 device also has an internal phase lock loop (PLL) controlled by the ROSC pin that can synchronize the switching cycle to the falling edge of an external system clock. 180° out-of-phase operation between two channels reduces input filter and power-supply induced noise.

The TPS563900 device has been designed for safe monotonic startup into pre-biased loads. The default start-up occurs when VIN is at 4.5 V (typical). The EN pin has an internal pullup current source that can be used to adjust the undervoltage lockout (UVLO) of the input voltage with two external resistors. In addition, the EN pin can be left floating in order to automatically start up the TPS563900 device with the internal pullup current.

The integrated MOSFETs of each channel allow for high-efficiency power-supply designs with continuous output currents up to 3.5 A. The MOSFETs have been sized to optimize efficiency for lower duty-cycle applications.

The TPS563900 device reduces the external component count by integrating the boot-recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and LX pins. The boot-capacitor voltage is monitored by a BOOT to LX UVLO (BOOT-LX UVLO) circuit which allows the LX pin to be pulled low in order to recharge the boot capacitor. The TPS563900 device operates at 100% duty cycle as long as the boot-capacitor voltage is higher than the preset BOOT-LX UVLO threshold which is 2.1 V (typical).

The TPS563900 device has a power-good comparator (PWRGD) with hysteresis that monitors the output voltage through the internal feedback voltage. The I^2C can read the power-good status with the commanding register.

The SS (soft-start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power up. A small value capacitor or resistor divider must be coupled to the pin for soft-start or critical power-supply sequencing requirements.

The TPS563900 device is protected from output overvoltage, overload, and thermal fault conditions. The TPS563900 device minimizes excessive-output overvoltage transients by taking advantage of the power good comparator. When the overvoltage comparator is activated, the high-side MOSFET turns off and is prevented from turning on until the internal feedback voltage is lower than 108% of the 0.6-V reference voltage. The TPS563900 device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protection which help control the inductor current and avoid current runaway. If the overcurrent condition has lasted for more than the hiccup wait time, the TPS563900 device shuts down and restarts after the hiccup time. The TPS563900 device also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 20°C (typical) below the thermal-shutdown trip point, the built-in thermal-shutdown hiccup timer is triggered. The TPS563900 device restarts under the control of the soft-start circuit automatically after the thermal-shutdown hiccup time is over.

Furthermore, if the overcurrent condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the TPS563900 device shuts down and restarts after the hiccup time, which is set for 16 384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

The TPS563900 device operates at any load condition unless the COMP-pin voltage drops below the COMP-pin start-switching threshold which is 0.25 V (typically).

When PSM mode operation is enabled, the TPS563900 device monitors the peak switch current of the high-side MOSFET. When the peak switch current is lower than 1 A (typical), the device stops switching in order to boost the efficiency until the peak switch current is higher than 1 A (typical) again.

DETAILED DESCRIPTION

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node (VOUT) to the FB pin. TI recommends to use divider resistors with a 1% tolerance or better.

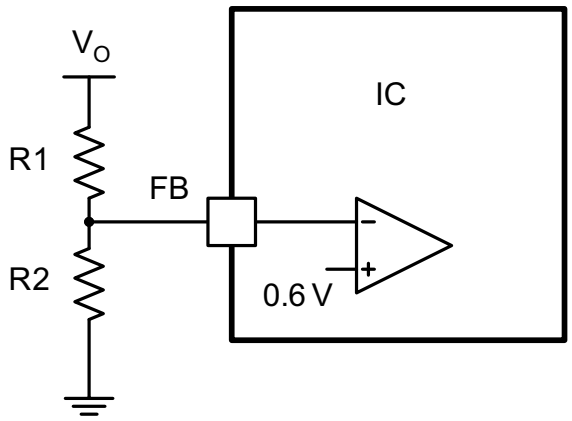

Figure 24. Voltage-Divider Circuit

$$R2 = R1 \times \left(\frac{0.6\ V}{V_O - 0.6\ V} \right) \quad (1)$$

Begin with R1 at 40.2-kΩ and use Equation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

The I^2C-controlled VID in a 7-bit register can also change the output voltage.

The minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) can limit the minimum and maximum output voltages (see Bootstrap Voltage (BOOT) and Low Dropout Operation).

Enabling and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN-pin voltage exceeds the threshold voltage, the device starts operation. If the EN-pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_Q state.

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The EN pin has an internal pullup current source which allows the user to float the EN pin to enable the device. If an application requires EN-pin control, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device disables when the VIN-pin voltage falls below the internal VIN-UVLO threshold. The internal VIN-UVLO threshold has a hysteresis of 500 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on PVIN, in split rail applications, configure the EN pin as shown in Figure 25.

When using the external UVLO function TI recommends to set the hysteresis to be greater than 500 mV.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated with Equation 2 and Equation 3.

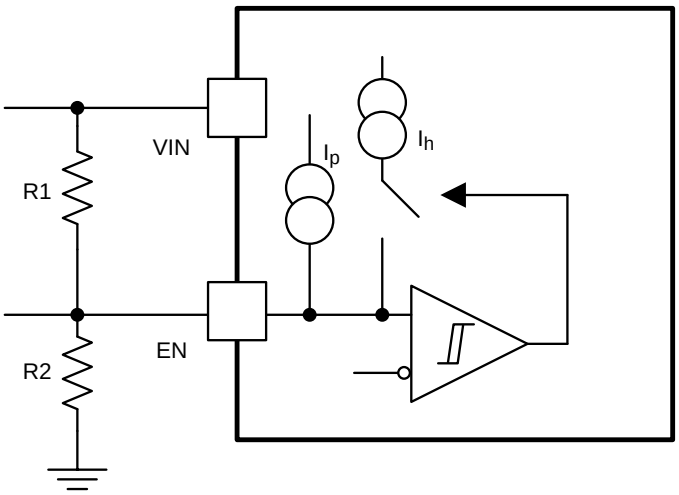

Figure 25. Adjustable VIN Under-Voltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R1(I_h + I_p)}$$

where

- I_h = 3 µA
- I_p = 3 µA
- $V_{ENrising}$ = 1.21 V
- $V_{ENfalling}$ = 1.17 V (3)

Adjustable Switching Frequency and Synchronization

Adjustable Switching Frequency and Synchronization mode overrides the resistor mode. The device is able to detect the proper mode automatically and switch from synchronization mode to resistor mode.

Adjustable Switching Frequency (Resistor Mode)

To determine the ROSC resistance for a given switching frequency, use Equation 4 or the curve in Figure 26. To reduce the solution size set the switching frequency as high as possible, however, tradeoffs of the supply efficiency and minimum controllable on time must be considered.

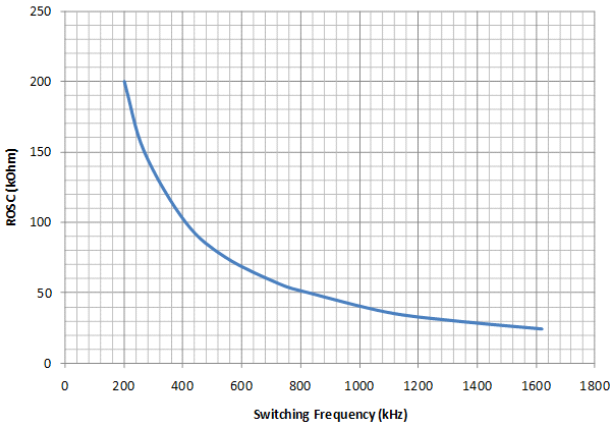

Figure 26. ROSC Versus Switching Frequency

$$\text{ROSC}\ (\text{k}\Omega) = 45580 \times f_{SW}^{-1.019}\ (\text{kHz}) \tag{4}$$

Synchronization

An internal phase-locked loop (PLL) has been implemented to allow synchronization between 200 kHz and 1600 kHz, and to easily switch from Resistor mode to Synchronization mode.

To implement the synchronization feature, connect a square-wave clock signal to the ROSC pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the falling edge of the ROSC pin.

In applications where both Resistor mode and Synchronization mode are required, configure the device as shown in Figure 27. Before the external clock is present, the device works in Resistor mode and the switching frequency is set by the ROSC resistor. When the external clock is present, the Synchronization mode overrides the Resistor mode. The first time the ROSC pin is pulled above the ROSC high threshold (2 V), the device switches from the Resistor mode to the Synchronization mode and the ROSC pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. Switching from the Synchronization mode back to the Resistor mode i snot recommended because the internal switching frequency first drops to 100 kHz before returning to the switching frequency set by the ROSC resistor.

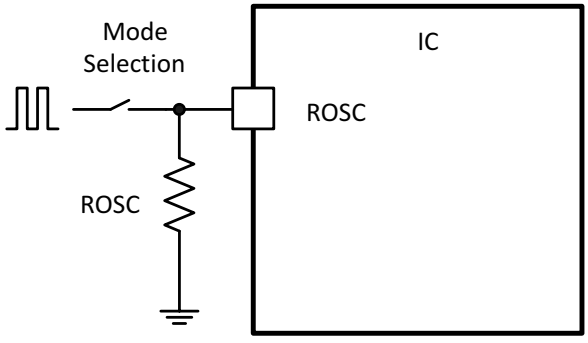

Figure 27. Resistor Mode and Synchronization Mode

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Soft-Start Time

The start up of the buck output is controlled by the voltage on the respective SS pin. When the voltage on the SS pin is less than the internal 0.6-V reference, the TPS563900 device regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6 V. The SS pin can be used to program an external soft-start function or to allow the output of the buck to track another supply during startup. The device has an internal pullup current source of 6 µA that charges an external soft-start capacitor to provide a linear ramping voltage at the SS pin. The TPS563900 device regulates the internal feedback voltage according to the voltage on the SS pin which allows V_O to rise smoothly from 0 V to the final regulated voltage. The total soft-start time is calculated with Equation 5 (approximately).

$$t_{SS}\ (ms) = C_{SS}\ (nF) \times \left(\frac{0.6 \times V}{6 \times \mu A} \right) \quad (5)$$

VID Control

When the I^2C is not in use, the output voltage of TPS563900 device is solely set by an external resistor divider. If the system must control the output voltage, the voltage-identification (VID) DAC can be controlled through the I^2C interface to the Output Voltage Selection register of 0x00H (Buck 1) and 0x1H (Buck 2). The output voltage is required to be preset by the external resistor divider. When the VID DAC is selected through the I^2C interface and the GO bit in the command register is set, the output voltage is set with the internal voltage divider over the external voltage divider.

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Out-of-Phase Operation

In order to reduce the input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This operation enables the system to have less input ripple to lower component cost, save board space, and reduce EMI.

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB-pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power-supply output voltage can respond faster than the error amplifier. When the power-supply output voltage responds faster than the error amplifier, a possibility of an output overshoot occurs. The OVP feature minimizes the overshoot by comparing the FB-pin voltage to the OVP threshold. If the FB-pin voltage is greater than the OVP threshold the high-side MOSFET turns off which prevents current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator. A small ceramic capacitor between the BOOT and LX pins provides the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT-pin voltage is less than VIN and the BOOT-LX voltage is below regulation. The value of this ceramic capacitor must be 0.1 µF. A ceramic capacitor with an X7R- or X5R-grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BOOT-LX-pin voltage is greater than the BOOT-LX UVLO threshold which is 2.1 V (typical). When the voltage between BOOT and LX drops below the BOOT-LX UVLO threshold, the high-side MOSFET turns off and the low-side MOSFET turns on which allows the boot capacitor to be recharged. In applications with split input voltage rails, 100% duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the COMP-pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and the current reference generated by the COMP-pin voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current of the low-side MOSFET is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally-set low-side sourcing current-limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current-limit is exceeded the low-side MOSFET turns off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP-pin voltage) occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16 384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C (typical). When the junction temperature drops below 140°C (typical), the internal thermal-hiccup timer begins to count. The device reinitiates the power-up sequence when the built-in thermal-shutdown hiccup time (16 384 cycles) is over.

Serial Interface Description

The I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All of the I^2C compatible devices connect to the I^2C bus through open-drain I/O pins, SDA, and SCL. A master device, typically a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives, transmits, or both receives and transmits data on the bus under control of the master device.

The TPS563900 device works as a slave and supports the following data transfer modes as defined in the I^2C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the power-supply solution which enables most functions to be programmed to new values based on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.5 V (typical).

The data transfer protocol for standard and fast modes is exactly the same, and therefore they are referred to as F/S-mode in this document. The TPS563900 device supports 7-bit addressing. The TPS563900 does not support 10-bit addressing and general call address.

The TPS563900 device has a 7-bit address with the two least-significant bits (LSB) bits set by the ADDR pin. Connecting ADDR to ground sets the address 0x60H, connecting ADDR to high sets the address 0x61H. Leaving this pin open sets the address 0x62H.

Table 1. I^2C Address Selection

ADDR PIN	I^2C ADDRESS
Connect to ground	0x60H
Open	0x61H
Connect to high	0x62H

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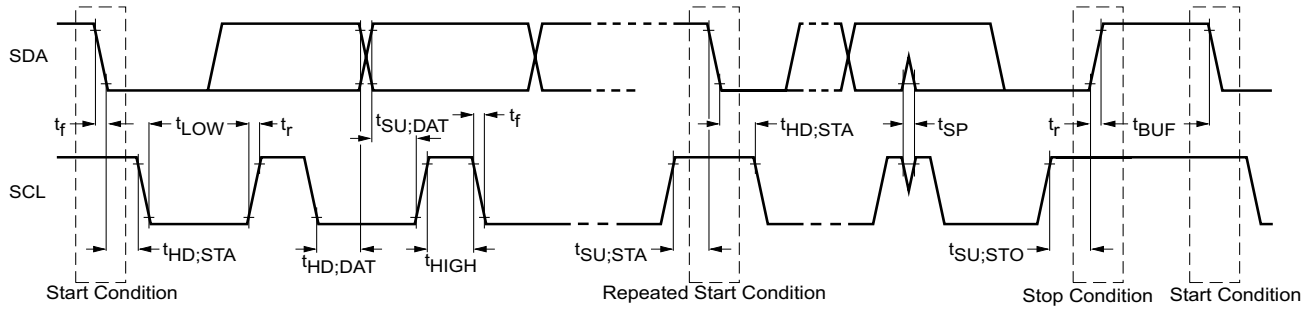

Figure 28. I²C Interface Timing Diagram

TPS563900 I²C Update Sequence

The TPS563900 device requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the TPS563900 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS563900 device. The TPS563900 device performs an update on the falling edge of the LSB byte.

When the TPS563900 device is in hardware shutdown (EN1 and EN2 pin tied to ground) the device cannot be updated through the I²C interface. Conversely, the I²C interface is fully functional during software shutdown (EN1 and EN2 bit = 0).

Figure 29. I²C Write Data Format

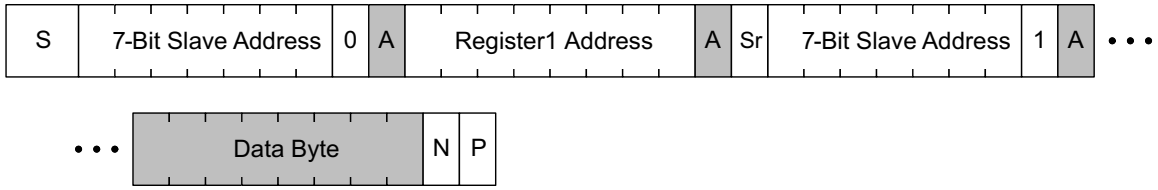

Figure 30. I²C Read Data Format

A: Acknowledge
N: Not Acknowledge
S: Start
P: Stop
Sr: Repeated Start

System Host
Chip

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Register Description

The following tables list the register descriptions.

Table 2. Register Addresses

NAME	BITS	ADDRESS
VOUT1_SEL	8	0x00H
VOUT2_SEL	8	0x01H
VOUT1_COM	8	0x02H
VOUT2_COM	8	0x03H
Sys_STATUS	8	0x04H

Table 3. VOUT1 Voltage Selection Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
VOUT1_SEL	7				10-mV step, from 0.68 V to 1.95 V
address: 0x00H	Bit 7	R/W	VOUT1_Bit7	0	GO bit, must be set '1' to enable I^2C voltage control
	Bit 6	R/W	VOUT1_Bit6	0	0x00H: 0.68 V; 0x7FH: 1.95 V
	Bit 5	R/W	VOUT1_Bit5	0	
	Bit 4	R/W	VOUT1_Bit4	0	
	Bit 3	R/W	VOUT1_Bit3	0	
	Bit 2	R/W	VOUT1_Bit2	0	
	Bit 1	R/W	VOUT1_Bit1	0	
	Bit 0	R/W	VOUT1_Bit0	0	

Table 4. VOUT2 Voltage Selection Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
VOUT2_SEL	7				10-mV step, from 0.68 V to 1.95 V
address: 0x01H	Bit 7	R/W	VOUT2_Bit7	0	GO bit, must be set '1' to enable I^2C voltage control
	Bit 6	R/W	VOUT2_Bit6	0	0x00H: 0.68 V; 0x7FH: 1.95 V
	Bit 5	R/W	VOUT2_Bit5	0	
	Bit 4	R/W	VOUT2_Bit4	0	
	Bit 3	R/W	VOUT2_Bit3	0	
	Bit 2	R/W	VOUT2_Bit2	0	
	Bit 1	R/W	VOUT2_Bit1	0	
	Bit 0	R/W	VOUT2_Bit0	0	

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Table 5. VOUT1 Command Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
VOUT1_COM	8				
address: 0x02H	Bit 7				Reserved
	Bit 6	R/W	Slew Rate 3	0	VOUT slew rate control. 000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16 cycles; 101: 10 mV/32 cycles; 110: 10 mV/64 cycles; 111: 10 mV/128 cycles
	Bit 5	R/W	Slew Rate 2	0	
	Bit 4	R/W	Slew Rate 1	0	
	Bit 3	R/W	Soft Discharge	0	0: Disable Soft Discharge 1: Enable Soft Discharge
	Bit 2	R/W	PSM Mode	0	00: select by MODE pin; 01: forced PWM mode; 10: auto PSM-PWM mode; 11: reserved
	Bit 1	R/W	PSM Mode	0	
	Bit 0	R/W	Disable1	0	0: output enabled; 1: output disabled

Table 6. VOUT2 Command Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
VOUT2_COM	8				
address: 0x03H	Bit 7				Reserved
	Bit 6	R/W	Slew Rate 3	0	VOUT slew-rate control. 000: 10 mV/cycle; 001: 10 mV/2 cycles; 010: 10 mV/4 cycles; 011: 10 mV/8 cycles; 100: 10 mV/16 cycles; 101: 10 mV/32 cycles; 110: 10 mV/64 cycles; 111: 10 mV/128 cycles
	Bit 5	R/W	Slew Rate 2	0	
	Bit 4	R/W	Slew Rate 1	0	
	Bit 3	R/W	Soft Discharge	0	0: Disable Soft Discharge 1: Enable Soft Discharge
	Bit 2	R/W	PSM Mode	0	00: select by MODE pin; 01: forced PWM mode; 10: auto PSM-PWM mode; 11: reserved
	Bit 1	R/W	PSM Mode	0	
	Bit 0	R/W	Disable2	0	0: output enabled; 1: output disabled

Table 7. System Status Register

	NUMBER OF BITS	ACCESS	NAME	DEFAULT VALUE	DESCRIPTION
SYS_STATUS	8				
address: 0x04H	Bit 7				Reserved
	Bit 6				Reserved
	Bit 5				Reserved
	Bit 4				Reserved
	Bit 3				Reserved
	Bit 2	R	Temperature Warning (> 125°C)	0	1: Die temperature over 125°C; 0: Die temperature below 125°C
	Bit 1	R	PGOOD2	0	0: VOUT2 in power good regulation range; 1: VOUT2 not in power good regulation range
	Bit 0	R	PGOOD 1	0	0: VOUT1 in power good regulation range; 1: VOUT1 not in power good regulation range

Table 8. Vout1 and Vout2 Output Voltage Setting

VOUT_SEL <6:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <6:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <6:0>	OUTPUT VOLTAGE (V)	VOUT_SEL <6:0>	OUTPUT VOLTAGE (V)
0	0.68	20	1	40	1.32	60	1.64
1	0.69	21	1.01	41	1.33	61	1.65
2	0.7	22	1.02	42	1.34	62	1.66
3	0.71	23	1.03	43	1.35	63	1.67
4	0.72	24	1.04	44	1.36	64	1.68
5	0.73	25	1.05	45	1.37	65	1.69
6	0.74	26	1.06	46	1.38	66	1.7
7	0.75	27	1.07	47	1.39	67	1.71
8	0.76	28	1.08	48	1.4	68	1.72
9	0.77	29	1.09	49	1.41	69	1.73
A	0.78	2A	1.1	4A	1.42	6A	1.74
B	0.79	2B	1.11	4B	1.43	6B	1.75
C	0.8	2C	1.12	4C	1.44	6C	1.76
D	0.81	2D	1.13	4D	1.45	6D	1.77
E	0.82	2E	1.14	4E	1.46	6E	1.78
F	0.83	2F	1.15	4F	1.47	6F	1.79
10	0.84	30	1.16	50	1.48	70	1.8
11	0.85	31	1.17	51	1.49	71	1.81
12	0.86	32	1.18	52	1.5	72	1.82
13	0.87	33	1.19	53	1.51	73	1.83
14	0.88	34	1.2	54	1.52	74	1.84
15	0.89	35	1.21	55	1.53	75	1.85
16	0.9	36	1.22	56	1.54	76	1.86
17	0.91	37	1.23	57	1.55	77	1.87
18	0.92	38	1.24	58	1.56	78	1.88
19	0.93	39	1.25	59	1.57	79	1.89
1A	0.94	3A	1.26	5A	1.58	7A	1.9
1B	0.95	3B	1.27	5B	1.59	7B	1.91
1C	0.96	3C	1.28	5C	1.6	7C	1.92
1D	0.97	3D	1.29	5D	1.61	7D	1.93
1E	0.98	3E	1.3	5E	1.62	7E	1.94
1F	0.99	3F	1.31	5F	1.63	7F	1.95

PRODUCT PREVIEW

APPLICATION INFORMATION

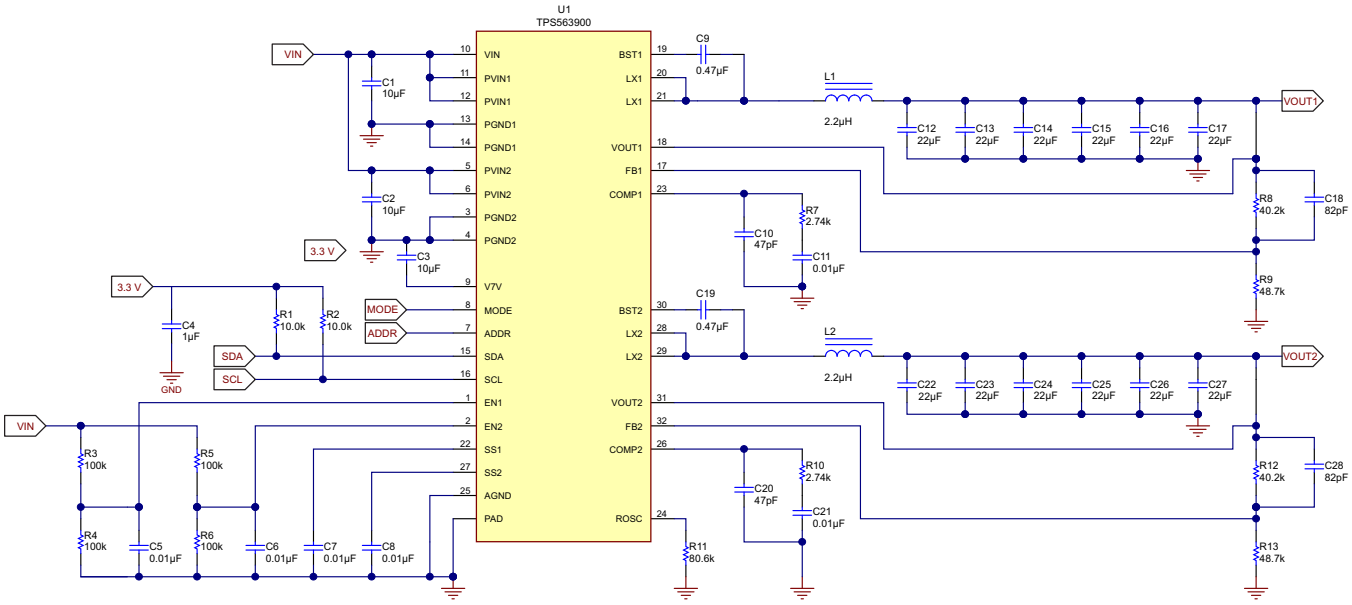


Figure 31. 1.1-V Output TPS563900 Design Example

Output Inductor Selection

To calculate the value of the output inductor, use Equation 6. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is typically from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_I max - V_O}{I_O \times LIR} \times \frac{V_O}{V_I max \times f_{SW}} \quad (6)$$

For the output filter inductor, not exceeding the RMS current and saturation current ratings is important. Use Equation 8 and Equation 9 to calculate the RMS and peak inductor current.

$$I_{rip} = \frac{V_I max - V_O}{L} \times \frac{V_O}{V_I max \times f_{SW}} \quad (7)$$

$$I_{L(RMS)} = \sqrt{I_O^2 + \frac{\left(\frac{V_O \times (V_I max - V_O)}{V_I max \times L \times f_{SW}}\right)^2}{12}} \quad (8)$$

$$I_{L(peak)} = I_O + \frac{I_{rip}}{2} \quad (9)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase the previously calculated peak-inductor current level. In transient conditions, the inductor current can increase up to the switch current-limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current-limit rather than the peak inductor current.

PRODUCT PREVIEW

Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor must supply the load with current when the regulator cannot. This situation occurs when desired hold-up times for the regulator occur where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current requirements of the load such as a transition from no load to full load. The regulator typically requires two or more clock cycles for the control loop in order to see the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 10 shows the minimum output capacitance necessary to accomplish this.

$$C_O = \frac{2 \times \Delta I_O}{f_{SW} \times \Delta V_O} \tag{10}$$

where

- ΔI_O is the change in output current
- f_{SW} is the regulators switching frequency
- ΔV_O is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in V_O for a load step of 3 A. For this example, ΔI_O = 3 A and ΔV_O = 0.05 × 3.3 = 0.165 V. Using these numbers gives a minimum capacitance of 75.8 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is typically small enough to ignore in this calculation.

Equation 11 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{Orip}}{I_{Orip}}} \tag{11}$$

where

- f_{SW} is the switching frequency
- V_{Orip} is the maximum allowable output voltage ripple
- I_{Orip} is the inductor ripple current

Equation 12 calculates the maximum ESR that an output capacitor can have to meet the output voltage ripple specification.

$$R_{ESR} < \frac{V_{Orip}}{I_{Orip}} \tag{12}$$

Additional capacitance deratings for aging, temperature, and DC bias must be factored in which increases this minimum value.

Capacitors generally have limits to the amount of ripple current that can be applied without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 13 calculates the RMS ripple current that the output capacitor must support.

$$I_{CO(RMS)} = \frac{V_O \times (V_I max - V_O)}{\sqrt{12} \times V_I max \times L \times f_{SW}} \tag{13}$$

PRODUCT PREVIEW

Input Capacitor Selection

The TPS563900 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10-µF of effective capacitance on the PVIN input-voltage pins. In some applications additional bulk capacitance can also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS563900 device. The input ripple current is calculated with Equation 14.

$$I_{I(RMS)} = I_O \times \sqrt{\frac{V_O}{V_I\,min} \times \frac{(V_I\,min - V_O)}{V_I\,min}} \tag{14}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations because of temperature is minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are typically selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. The TPS563900 device can operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple is calculated with Equation 15.

$$\Delta V_I = \frac{I_O\,max \times 0.25}{C_I \times f_{SW}} \tag{15}$$

PRODUCT PREVIEW

Loop Compensation

The integrated-buck DC-DC converter in the TPS563900 device incorporates a peak current-mode control scheme. The error amplifier is a transconductance amplifier with a gain of 1350 µA/V. A typical type-II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow the following steps.

1. Select the switching frequency, f_{sw}, that is appropriate for the application based on L and C sizes, output ripple, EMI, and others. A switching frequency between 500 kHz to 1 MHz gives the best trade off between performance and cost. To optimize efficiency, lowering switching frequency is desired.
2. Set up crossover frequency, f_c, which is typically between 1/5 and 1/20 of f_{SW}.
3. R_C is calculated with Equation 16.

$$R_C = \frac{2\pi \times f_C \times V_O \times C_O}{g_m \times V_{ref} \times gm_{ps}} \quad (16)$$

where

- g_m is the error amplifier gain (1350 µA/V)
- gm_{ps} is the power stage voltage to current conversion gain (10 A/V)

4. Calculate C_C by placing a compensation zero at or before the dominant pole as shown in Equation 17.

$$(f_P = \frac{1}{C_O \times R_L \times 2\pi}) \times s \quad (17)$$

$$C_C = \frac{R_L \times C_O}{R_C} \quad (18)$$

5. The optional C_b is used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times C_O}{R_C} \quad (19)$$

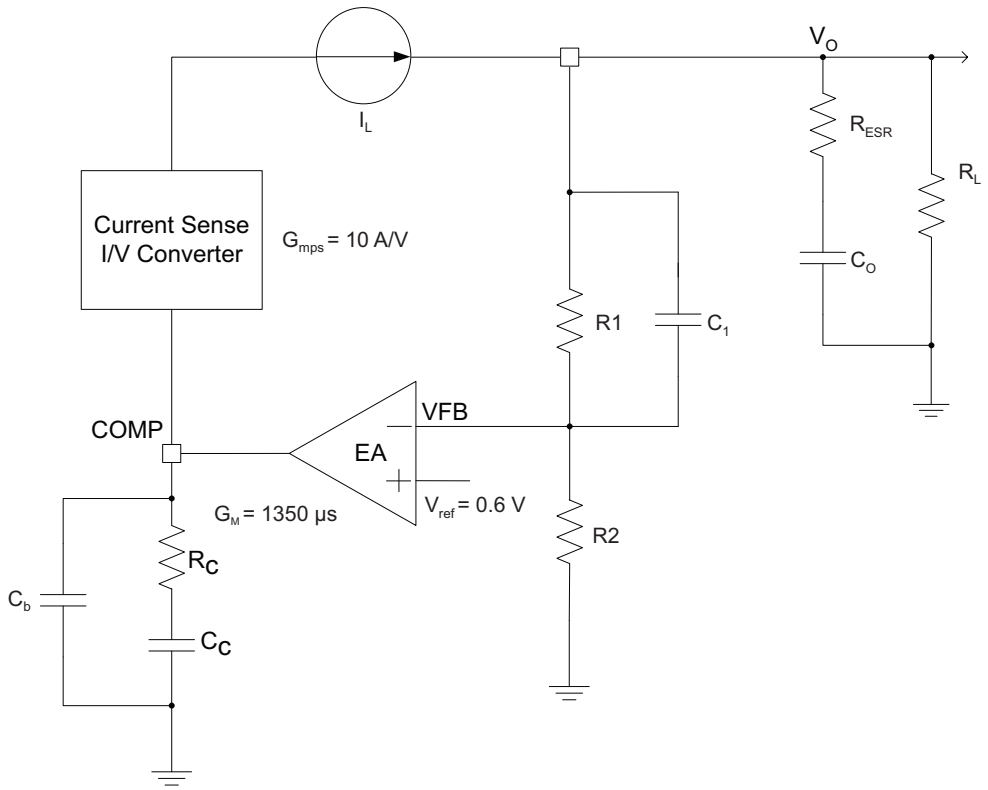


Figure 32. DC-DC Loop Compensation

PRODUCT PREVIEW

PCB Layout Guideline

Figure 33 shows the 2-layer PCB layout for the TPS563900 device.

Layout is a critical portion of good power-supply design. See Figure 33 for a PCB layout example. The top layer contains the main power traces for VIN, VOUT, and VLX. Also on the top layer are connections for the remaining pins of the TPS563900 and a large top-side area filled with ground. The top-layer ground area must be connected to the internal ground layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS563900 device to provide a thermal path from the exposed thermal-pad land to ground. The bottom layer acts as ground plane that connects the analog ground and power ground.

The GND pin must be tied directly to the exposed thermal pad under the IC and the power pad. For operation at a full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipating area. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin must be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care must be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.

The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output-filter capacitor ground must use the same power-ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The additional external components can be placed approximately as shown.

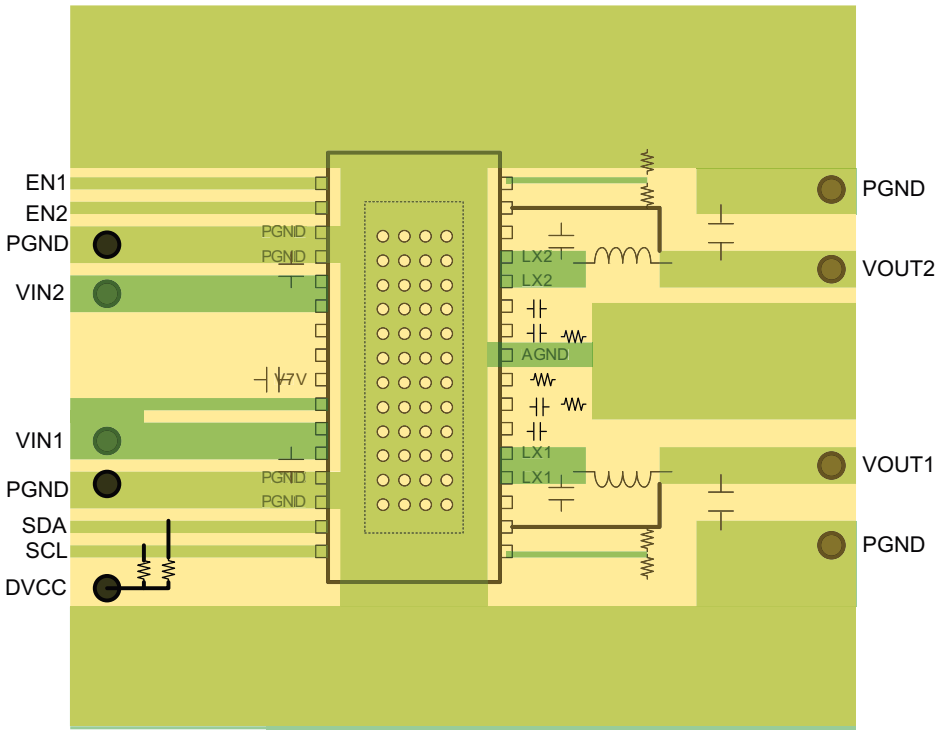


Figure 33. TPS563900 Layout on 2-layer PCB

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS563900DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS563900	Samples
TPS563900DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS563900	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

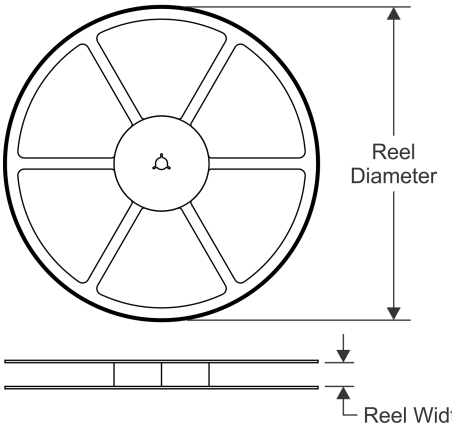
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

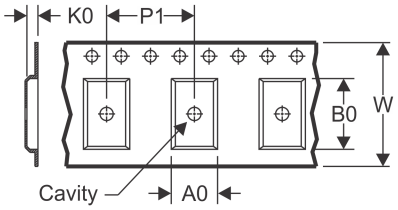
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

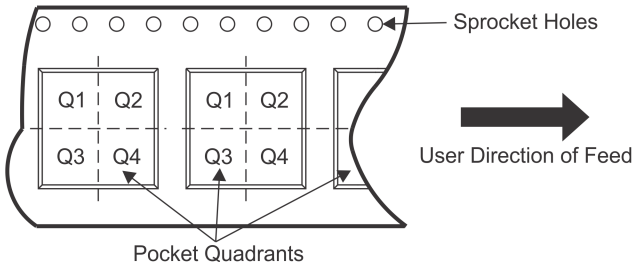


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

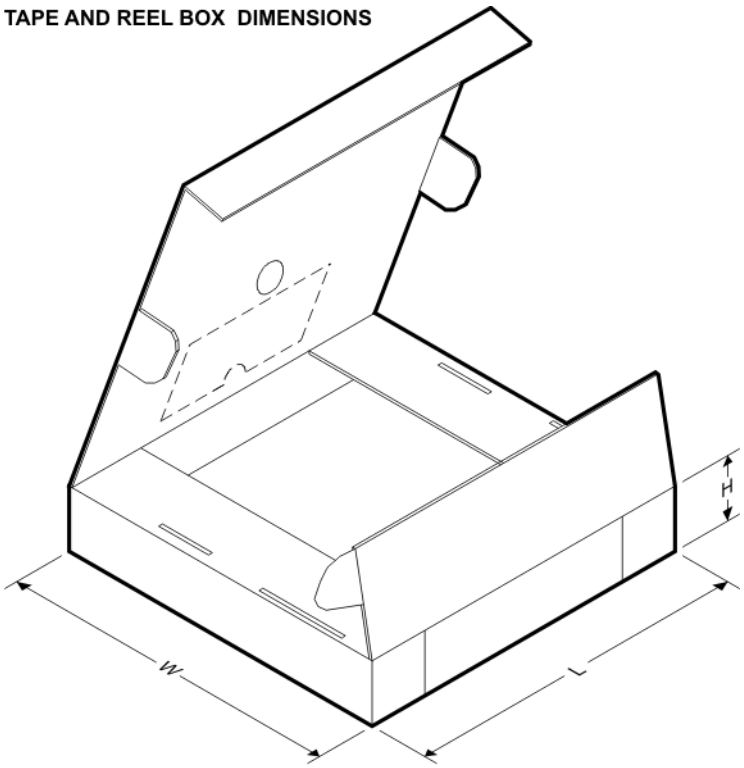
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563900DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

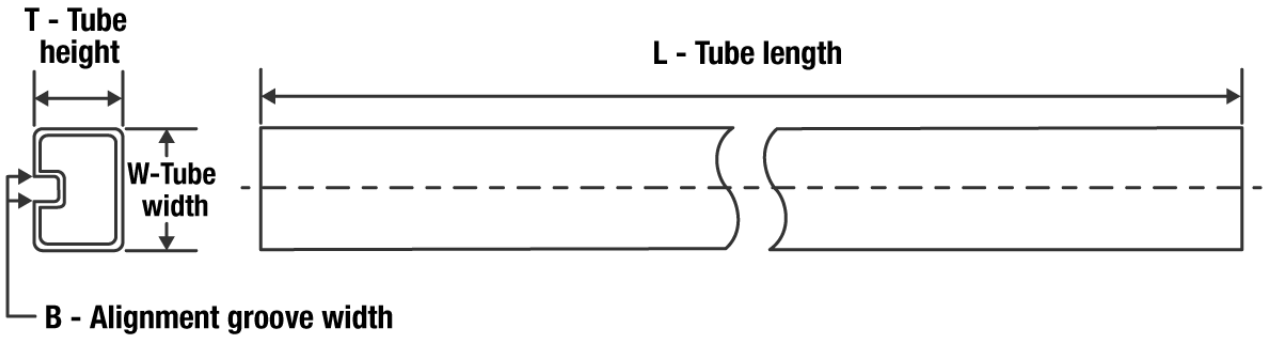
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563900DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS563900DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

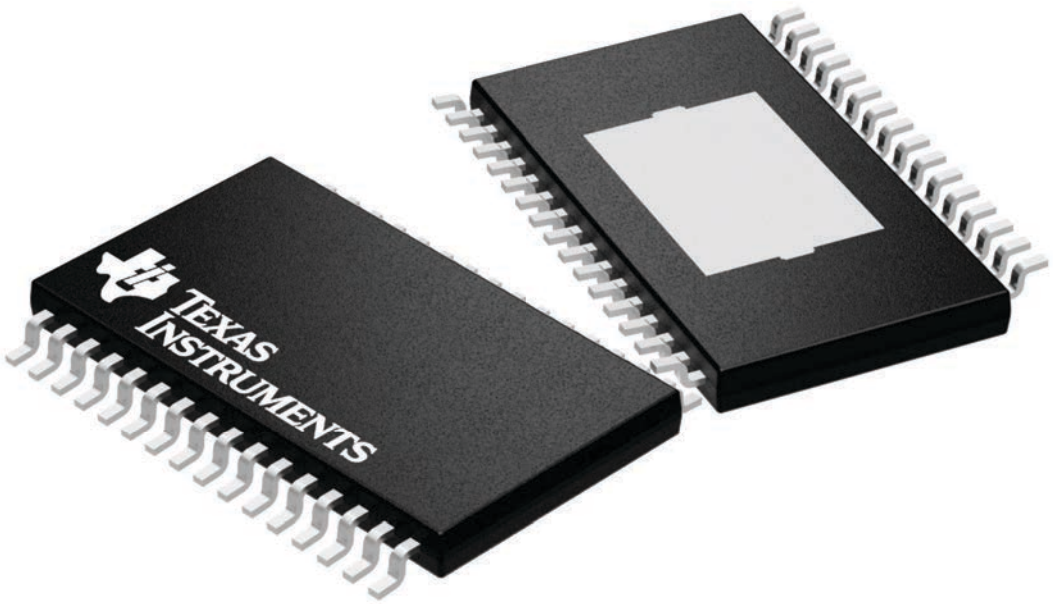
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

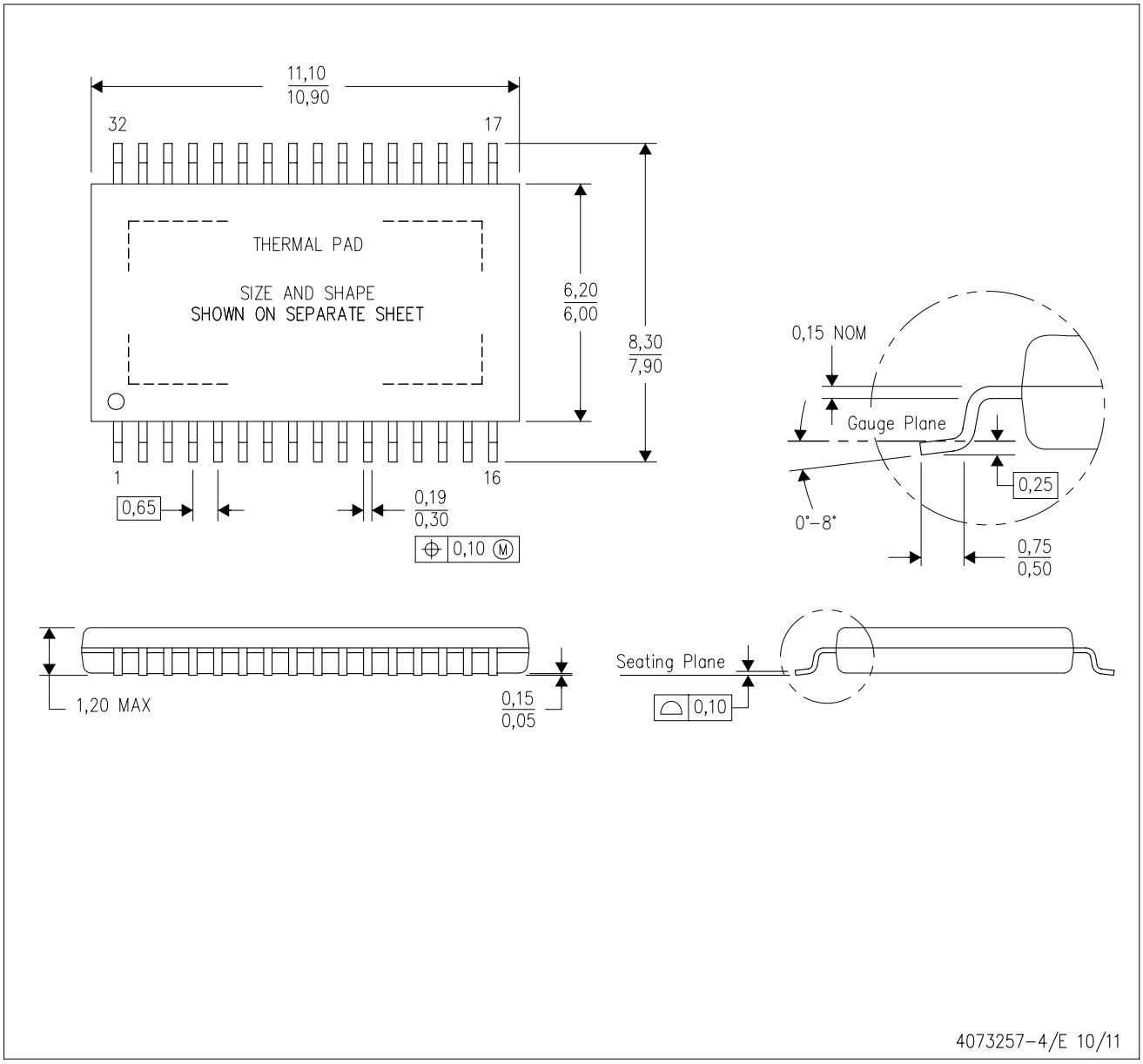
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

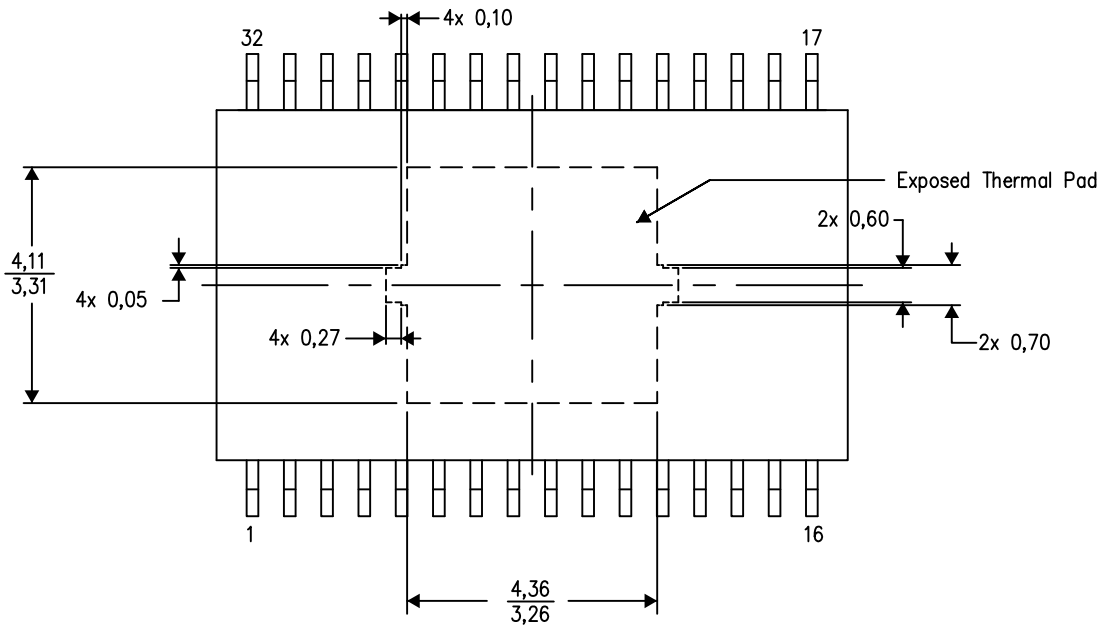
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

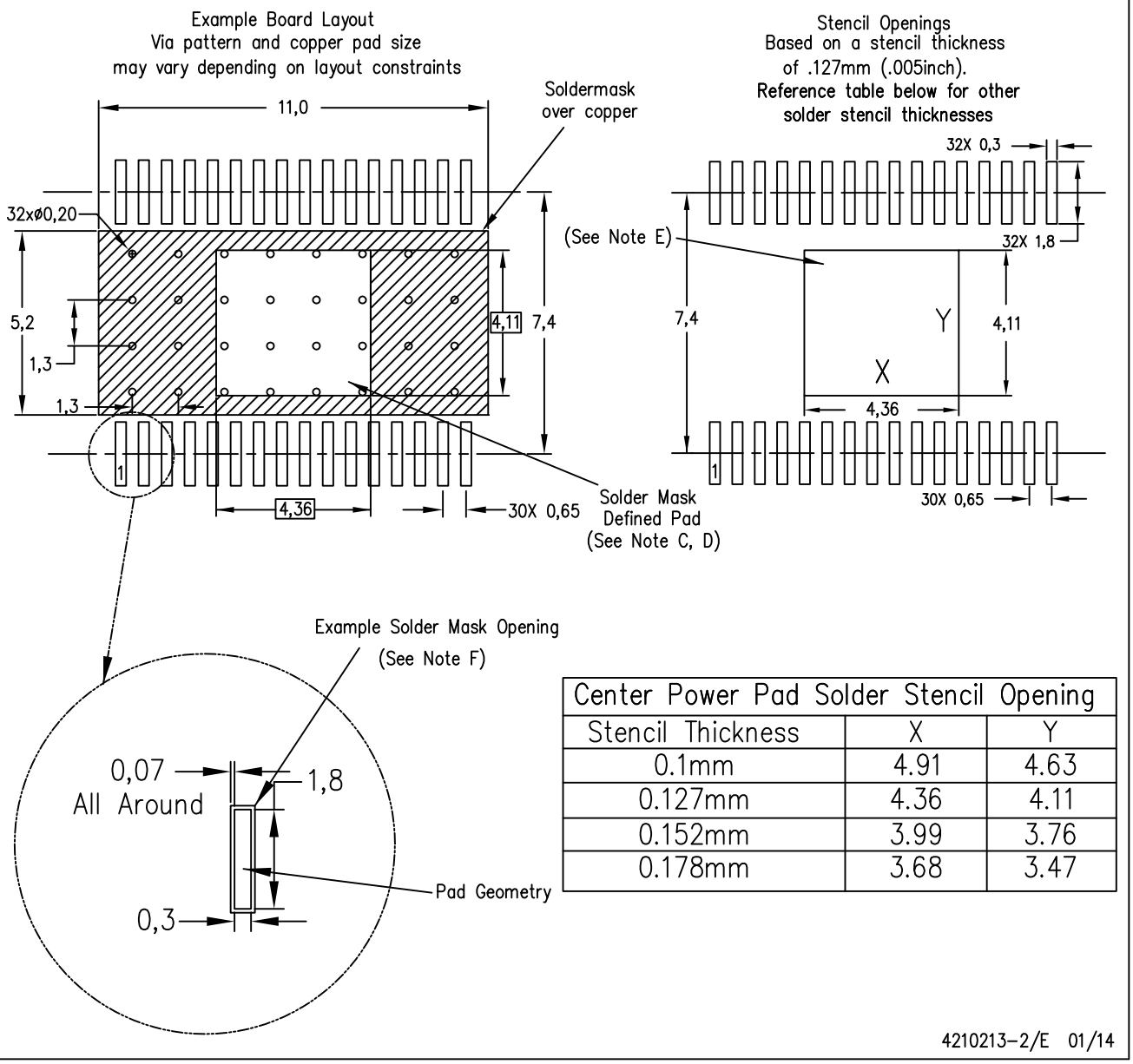
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

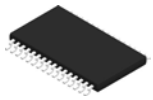
PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

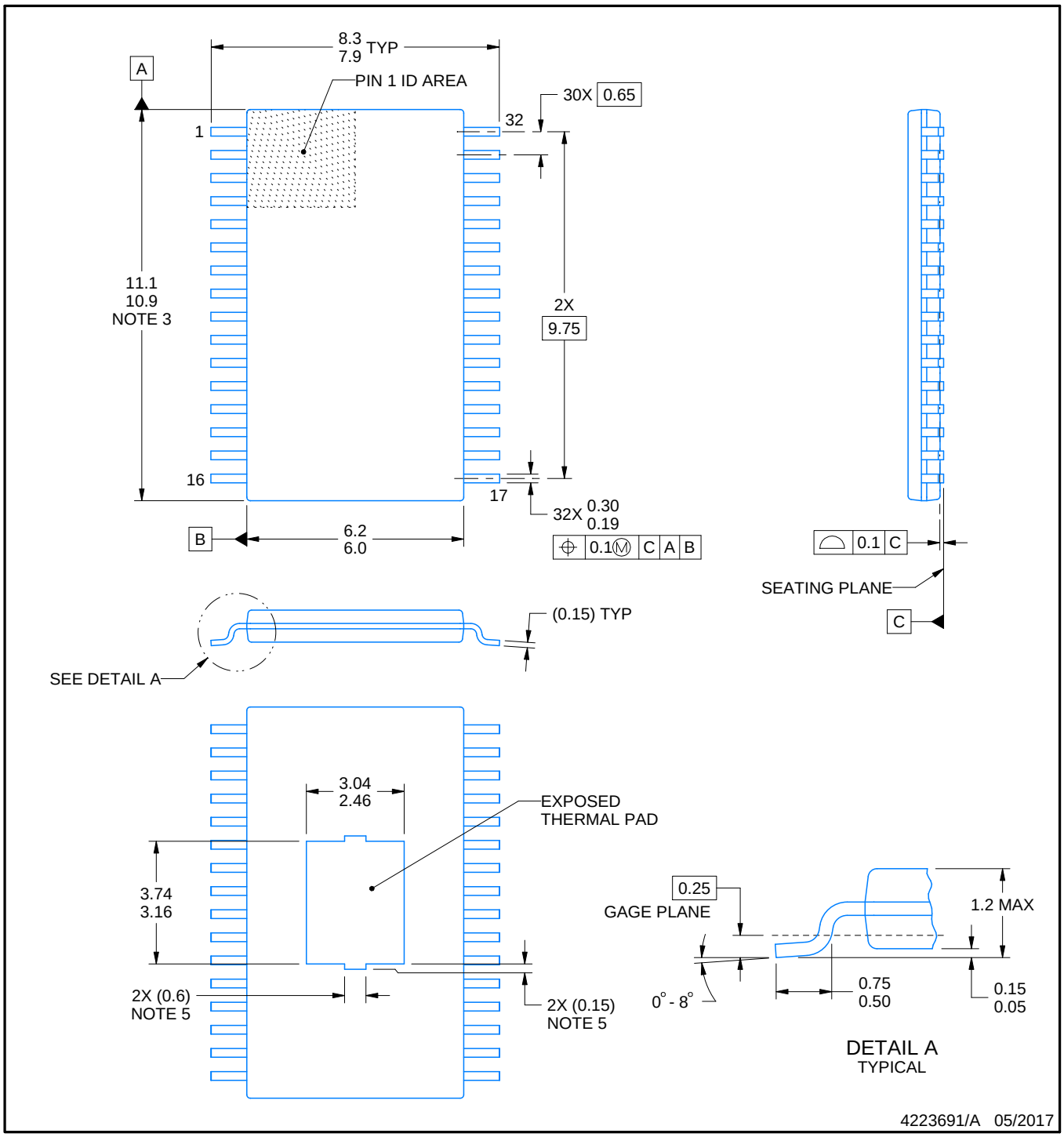


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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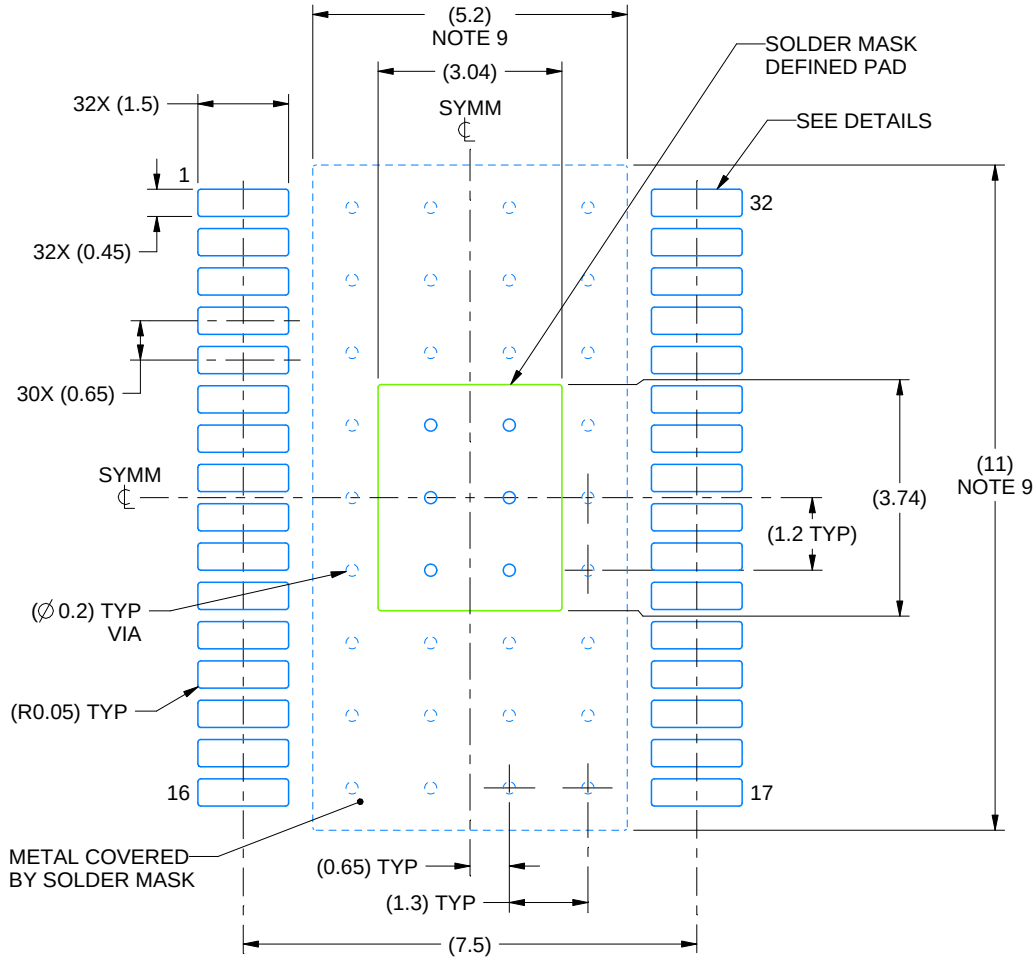
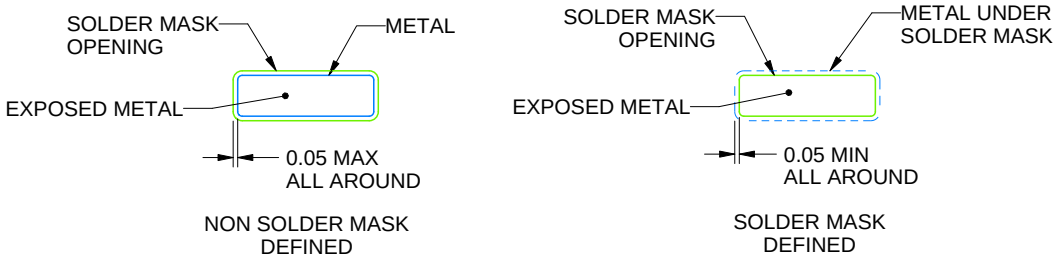
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

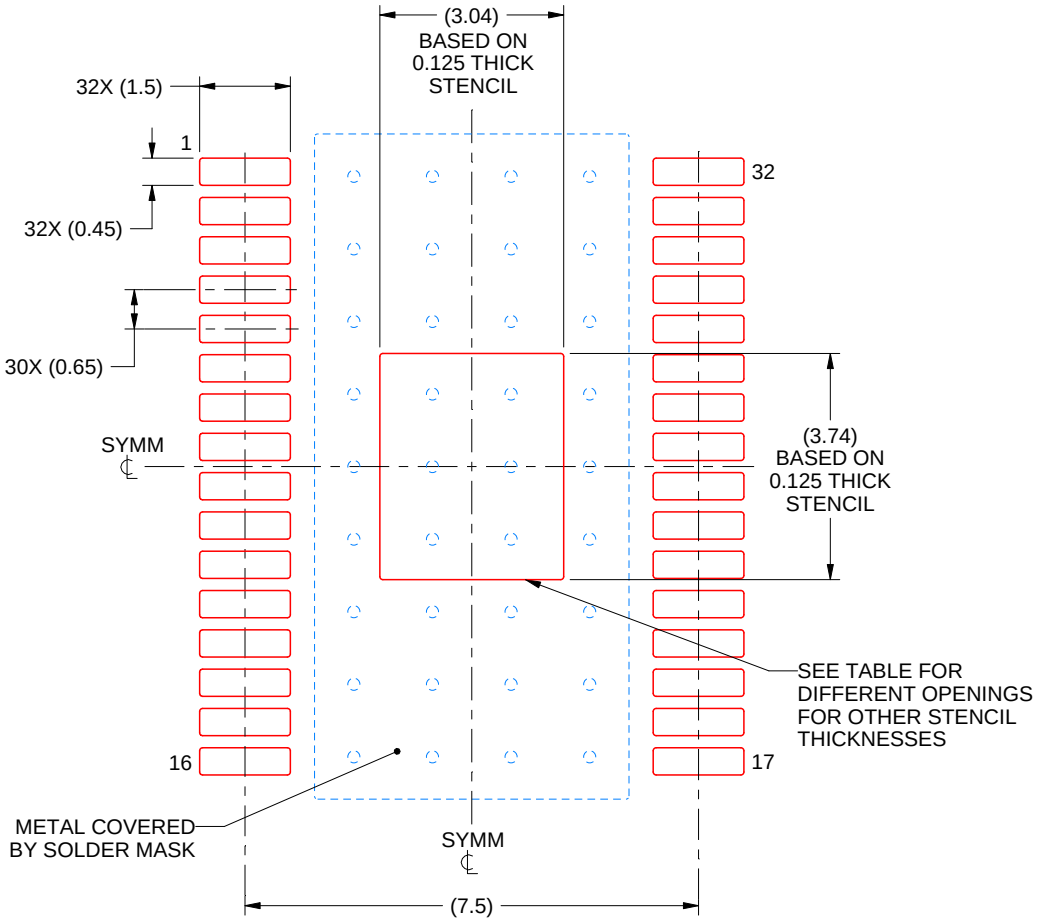


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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