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APPLICATION NOTE 474 Precision DAC and Watchdog Improve Analog Output Safety

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Abstract: Using a DAC and a microprocessor supervisor, the system safety can be improved in industrial controllers, programmable-logic controllers (PLC), and data-acquisition systems. The analog output is set to zero-scale (or pin-programmable midscale) when a microprocessor failure, optocoupler failure, or undervoltage condition occurs. A simple application is shown on how to implement this function.

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Introduction

The need for safe states in industrial applications is critical when system-level failures occur. A feature-rich precision digital-to-analog converter (DAC) and microprocessor (μ P) supervisory circuit with watchdog timer can be used to assure that analog outputs default to a known midscale or zero-scale level.

Circuit Operation

Common analog-output control signals used in industrial controllers, programmable-logic controllers (PLCs), and data-acquisition systems (DAS) include voltage outputs such as 0 to 5V, 0 to 10V, \pm 5V, \pm 10V, and 4–20mA current loop. To ensure safety integrity, the analog-output control signal should default to a known midscale or zero-scale safe state in response to a μ P or system failure. For additional safety, analog output modules often employ optocouplers to provide galvanic isolation between the μ P and analog output signals.

Requirements for analog output safety and reliability are met by the **Figure 1** circuit. When a μ P failure, optocoupler failure, or undervoltage condition occurs, the supervisory circuit (U3, the MAX6303) sets the 12-bit DAC (U2, the MAX5120) analog output to mid-scale, which in turn sets V_{OUT} to 0V safe-state output. This circuit also improves mean time between failure (MTBF) by reducing the number of I/O pins at the μ P and by eliminating an optocoupler.



Figure 1. When a failure occurs in the supply voltage, optocouplers, or μ P operation, this DAC (U2) and μ P supervisor (U3) together generate a user-programmed, safe-state default output (V_{OUT}).

Three DAC features enable the circuit to meet the safety-critical functions: an asynchronous reset input (active-low CLR), a user-selectable reset-value input (RSTVAL), and a user-programmable output (UPO). These built-in features also eliminate the need for an optocoupler, reduce the number of I/O pins at the μ P, and eliminate external discrete circuitry. The μ P supervisor includes a resistor-programmable reset input threshold, a capacitor-programmable watchdog timer, and a reset timeout period.

Here is how the circuit works. As DAC codes range from 000hex to FFFhex, the analog output voltage (V_{OUT}) ranges from -10V to +10V. Op amp U1A (MAX9944) is offset by the DAC's internal 10ppm/°C precision bandgap reference; output op amp U1B (MAX9944) is configured as a buffer with a gain of 4.

Output voltage for the circuit is calculated as:

$$V_{OUT} = V_{REF} \times (G \times NB/4096 - 1) \times (R_F/R_{IN} + 1)$$
 (Eq. 1)

Where NB is the numeric value of the DAC's binary code; V_{REF} is the internal reference voltage; G is the gain of U1A; and R_F/R_{IN} is U1B's gain-resistor ratio.

Microprocessor supervisor U3 monitors the isolated supply voltage (VISO) through its V_{CC} pin. It also monitors µP

activity at the WDI pin with UPO and generates a reset output command through active-low RESET. A resistordivider at RESET IN (U3 pin 1) determines the reset-level voltage threshold (V_{TH}). Similarly, the reset timeout period (t_{RP}) and watchdog timeout period (t_{WD}) are determined by capacitor values at SRT and SWT. Connect WDS to V_{CC} to enter extended mode, lengthening t_{WD} by a factor of 500. The following equations calculate values needed in the circuit:

$$V_{RST} = V_{TH}(R1 + R2)/R2$$
 (Eq. 2)

Where $V_{TH} = 1.22V$ and V_{RST} is the adjustable reset threshold voltage:

$C_{SRT} = t_{RP}/2.67 $ (Eq.	. :	3	3))
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Where C_{SRT} is in pF and t_{RP} is in μ s; C_{SWT} is in pF and t_{WD} is in μ s. Therefore:

 $C_{SWT} = t_{WD} / (500 \times 2.67)$ (Eq. 4)

If V_{CC} fails or if the μ P cannot toggle WDI via UPO, then U3 asserts the active-low RESET output which resets U2 through its CLR input. This action resets U2's output to the condition set by RSTVAL (to midscale in this case, which produces 0V at V_{OUT}). In normal operation the μ P must update U2 at intervals less than the programmed watchdog timeout period (t_{WD}). In this manner the UPO output routinely toggles WDI, meaning that UPO "kicks the dog" at WDI. Note that after the reset timeout period (t_{RP}), active-low RESET releases CLR but the DAC output remains at midscale until updated.

The switch between U3's RESET IN and GND terminals allows the user to command an emergency shutdown. Other devices to consider for the watchdog function are the MAX6316 series and the MAX6369 series, both of which offer fixed timeout periods and are available in SOT23 packages. Also, the DAC's unipolar and bipolar modes allow it to produce all common analog-output control signals.

Conclusion

Improvements to safety integrity can be realized with the special features of a precision DAC and watchdog timer μP supervisor. Together these devices can provide safe state operating conditions for the analog outputs used in many industrial-controller applications.

Related Parts		
MAX5120	+3V/+5V, 12-Bit, Serial, Voltage-Output DACs with Internal Reference	Free Samples
MAX5725	Ultra-Small, Octal-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface	Free Samples
MAX5825	Ultra-Small, Octal Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I ² C Interface	Free Samples
MAX6303	+5V, Low-Power, μP Supervisory Circuits with Adjustable Reset/Watchdog	Free Samples
MAX6316	5-Pin μP Supervisory Circuits with Watchdog and Manual Reset	Free Samples

MAX6369	Pin-Selectable Watchdog Timers	Free Samples
MAX9944	High-Voltage, Precision, Low-Power Op Amps	Free Samples

More Information

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