LM3205 650mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

Check for Samples: LM3205

FEATURES

- **2 MHz (typ.) PWM Switching Frequency**
- **Operates from a Single Li-Ion Cell (2.7V to 5.5V)**
- **Variable Output Voltage (0.8V to 3.6V)**
- **Fast Output Voltage Transient (0.8V to 3.6V in 20µs)**
- **650mA Maximum Load Capability**
- **High Efficiency (96% Typ at 4.2V_{IN}, 3.4V_{OUT} at 400mA) from Internal Synchronous Rectification**
- **Current Overload Protection**
- **Thermal Overload Protection**
- **Packages**
  - **8-Pin DSBGA (Lead Free)**
- **10-Pin WSON**

APPLICATIONS

- **Cellular Phones**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery Powered RF Devices**

DESCRIPTION

The LM3205 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell, however they may be used in many other applications. It steps down an input voltage from 2.7V to 5.5V to a variable output voltage from 0.8V(typ.) to 3.6V(typ.). Output voltage is set using a V_{CON} analog input for controlling power levels and efficiency of the RF PA.

The LM3205 offers superior performance for mobile phones and similar RF PA applications. Fixed-frequency PWM operation minimizes RF interference. Shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ.).

The LM3205 is available in DSBGA package and WSON package. For all other package options contact your local TI sales office.

A high switching frequency (2 MHz) allows use of tiny surface-mount components. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

TYPICAL APPLICATION

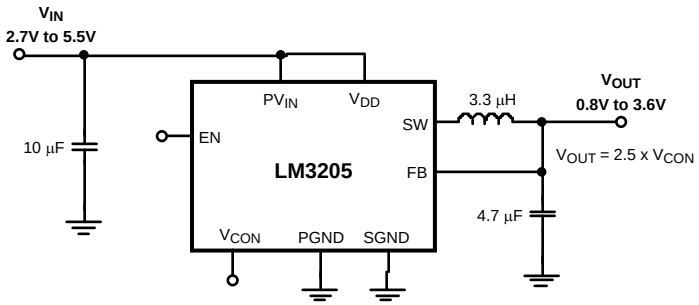


Figure 1. LM3205 Typical Application

CONNECTION DIAGRAMS

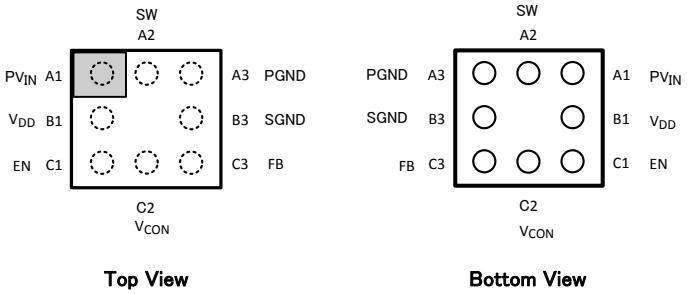


Figure 2. 8–Bump Thin DSBGA Package, Large Bump
NS Package Number YZR0008GNA

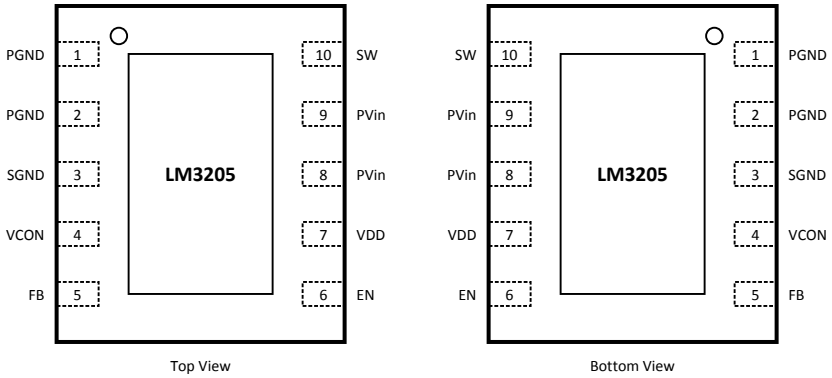


Figure 3. 10–Pin WSON
NS Package Number DSC0010A

PIN DESCRIPTIONS

Pin #		Name	Description
DSBGA	WSON		
A1	8, 9	PV_{IN}	Power Supply Voltage Input to the internal PFET switch.
B1	7	V_{DD}	Analog Supply Input.
C1	6	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
C2	4	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	5	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
B3	3	SGND	Analog and Control Ground
A3	1, 2	PGND	Power Ground
A2	10	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3205.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

V_{DD}, PV_{IN} to SGND		−0.2V to +6.0V
PGND to SGND		−0.2V to +0.2V
EN, FB, V_{CON}		(SGND −0.2V) to (V_{DD} +0.2V) w/6.0V max
SW		(PGND −0.2V) to (PV_{IN} +0.2V) w/6.0V max
PV_{IN} to V_{DD}		−0.2V to +0.2V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)		+260°C
ESD Rating(5)(6)	Human Body Model	2 kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3205 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(5) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200pF capacitor discharged directly into each pin.
(6) TI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling techniques can result in damage.

OPERATING RATINGS(1)(2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0mA to 650mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3205 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal DSBGA	100°C/W
Resistance (θ_{JA}), DSBGA YZR08 Package(1)	
Junction-to-Ambient Thermal WSON	55°C/W
Resistance (θ_{JA}), WSON DSC0010A Package(1)	

(1) **DSBGA:** Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. A 4 layer, 4" x 4", 2/1/1/2 oz. Cu board as per JEDEC standards is used for the measurements. **WSON:** The value of (θ_{JA}) in WSON-10 could fall in a range of 50°C/W to 150°C/W (if not wider), depending on PWB material, layout, and environmental conditions. In applications where high maximum power dissipation exits (high V_{IN} , high I_{OUT}), special care must be paid to thermal dissipation areas. For more information on these topics for WSON, refer to **Application Note 1187: Leadless Leadframe Package (LLP)** (SNOA401) and the **Power Efficiency and Power Dissipation** section of this datasheet

ELECTRICAL CHARACTERISTICS[1][2][3]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, all specifications apply to LM3205TL/LM3205SD with: $PV_{IN} = V_{DD} = EN = 3.6V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ MIN}$	Feedback Voltage at minimum setting	$V_{CON} = 0.32V$[3]	**0.75**	0.8	**0.85**	V
$V_{FB,\ MAX}$	Feedback Voltage at maximum setting	$V_{CON} = 1.44V$, $V_{IN} = 4.2V$[3]	**3.537**	3.6	**3.683**	V
I_{SHDN}	Shutdown supply current	EN = SW = V_{CON} = 0V[4]		0.01	**2**	µA
I_Q	DC bias current into V_{DD}	V_{CON} = 2V, FB = 0V, No Switching[5]		1	**1.4**	mA
$R_{DSON(P)}$ *DSBGA*	Pin-pin resistance for PFET	I_{SW} = 200mA		140	200 **230**	mΩ
$R_{DSON(N)}$ *DSBGA*	Pin-pin resistance for NFET	I_{SW} = -200mA		300	415 **485**	mΩ
$R_{DSON(P)}$*WSON*	Pin-pin resistance for PFET	I_{SW} = 200mA		170	230 **260**	mΩ
$R_{DSON(N)}$*WSON*	Pin-pin resistance for NFET	I_{SW} = -200mA		330	445 **515**	mΩ
$I_{LIM,PFET}$	Switch peak current limit	See[6]	**935**	1100	**1200**	mA
F_{OSC}	Internal oscillator frequency		**1.7**	2	**2.3**	MHz
$V_{IH,EN}$	Logic high input threshold		**1.2**			V
$V_{IL,EN}$	Logic low input threshold				**0.5**	V
$I_{PIN,EN}$	Pin pull down current			5	**10**	µA
Z_{CON}	V_{CON} input resistance		100			kΩ
Gain	V_{CON} to V_{OUT} Gain	$0.32V \le V_{CON} \le 1.44V$		2.5		V/V

(1) All voltages are with respect to the potential at the GND pins. The LM3205 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.

(3) The parameters in the electrical characteristics table are tested under open loop conditions at $PV_{IN} = V_{DD} = 3.6V$. For performance over the input voltage range and closed loop results refer to the datasheet curves.

(4) Shutdown current includes leakage current of PFET.

(5) I_Q specified here is when the part is operating at 100% duty cycle.

(6) Current limit is built-in, fixed, and not adjustable. Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

SYSTEM CHARACTERISTICS

The following spec table entries are specified by design providing the component values in the typical application circuit are used. **These parameters are not specified by production testing.** Min and Max limits apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ 85°C) and over the V_{IN} range = 2.7V to 5.5V, T_A = 25°C, PV_{IN} = V_{DD} = EN = 3.6V, L = 3.3µH, DCR of L ≤ 100mΩ, C_{IN} = 10µF, 0603, 6.3V (4.7µF||4.7µF, 0603, 6.3V can be used), C_{OUT} = 4.7µF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0.8V to 3.6V	V_{IN} = 4.2V, C_{OUT} = 4.7µF, L = 3.3µH, R_{LOAD} = 5.5Ω		20	30	µs
	Time for V_{OUT} to fall from 3.6V to 0.8V	V_{IN} = 4.2V, C_{OUT} = 4.7µF, L = 3.3µH, R_{LOAD} = 10Ω		20	30	µs
C_{CON}	V_{CON} input capacitance	V_{CON} = 1V, Test frequency = 100 kHz			20	pF
Linearity	Linearity in control range 0.32V to 1.44V	V_{IN} = 3.9V Monotonic in nature	-3		+3	%
I_{CON}	Control pin input current		-10		10	µA
T_{ON}	Turn on time (time for output to reach 3.6V from Enable low to high transition)	EN = Low to High, V_{IN} = 4.2V, V_O = 3.6V, C_{OUT} = 4.7µF, I_{OUT} ≤ 1mA		70	100	µs
η	Efficiency (L = 3.3µH, DCR ≤ 100mΩ)	V_{IN} = 3.6V, V_{OUT} = 0.8V, I_{OUT} = 90mA		83		%
		V_{IN} = 4.2V, V_{OUT} = 3.4V, I_{OUT} = 400mA		96		%
V_{OUT}_ripple	Ripple voltage, PWM mode	V_{IN} = 3V to 4.5V, V_{OUT} = 0.8V, I_{OUT} = 10mA to 400mA(1)		10		mVp-p
Line_tr	Line transient response	V_{IN} = 600mV perturbance, T_{RISE} = T_{FALL} = 10µs, V_{OUT} = 0.8V, I_{OUT} = 100mA		50		mVpk
Load_tr	Load transient response	V_{IN} = 3.1/3.6/4.5V, V_{OUT} = 0.8V, transients up to 100mA, T_{RISE} = T_{FALL} = 10µs		50		mVpk
PSRR	V_{IN} = 3.6V, V_{OUT} = 0.8V, I_{OUT} = 100mA	sine wave perturbation frequency = 10kHz, amplitude = 100mVp-p		40		dB

(1) Ripple voltage should measured at C_{OUT} electrode on good layout PC board and under condition using suggested inductors and capacitors.

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit in Figure 31, $PV_{IN} = V_{DD}$ = EN = 3.6V, L = 3.3uH, DCR of L ≤ 100mΩ, C_{IN} = 10uF, 0603, 6.3V (4.7uF||4.7uF, 0603, 6.3V can be used), C_{OUT} = 4.7uF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted)

Quiescent Current vs Supply Voltage (V_{CON} = 2V, FB = 0V, No Switching)

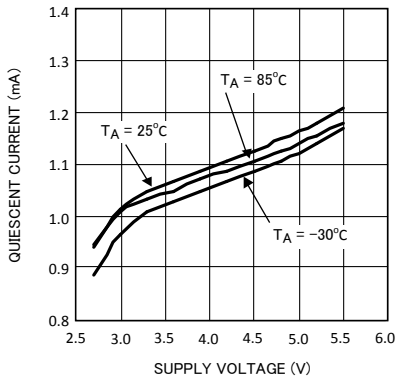


Figure 4.

Shutdown Current vs Temperature (V_{CON} = 0V, EN = 0V)

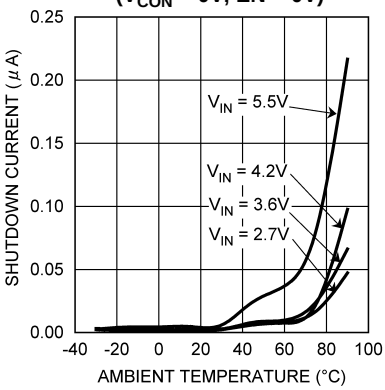


Figure 5.

Switching Frequency Variation vs Temperature (V_{OUT} = 1.3V, I_{OUT} = 200mA)

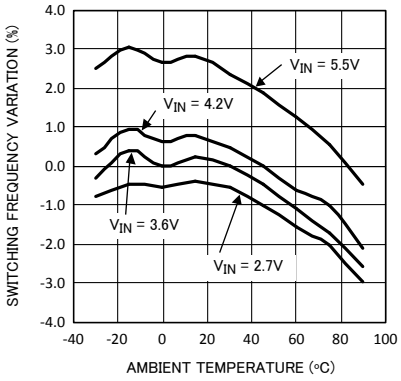


Figure 6.

Output Voltage vs Supply Voltage (V_{OUT} = 1.3V)

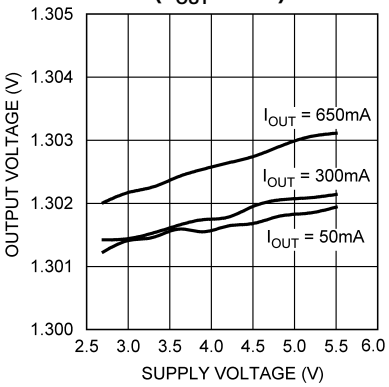


Figure 7.

Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 0.8V)

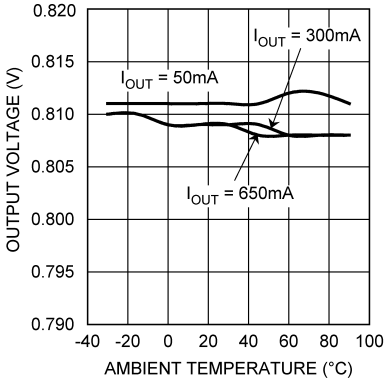


Figure 8.

Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 3.4V)

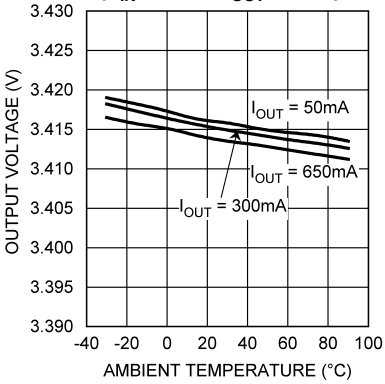


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, PV_{IN} = V_{DD} = EN = 3.6V, L = 3.3uH, DCR of L ≤ 100mΩ, C_{IN} = 10uF, 0603, 6.3V (4.7uF||4.7uF, 0603, 6.3V can be used), C_{OUT} = 4.7uF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted)

Open/Closed Loop Current Limit vs Temperature (PWM mode)

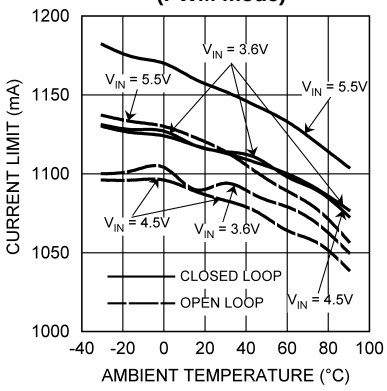


Figure 10.

V_{CON} Voltage vs Output Voltage (V_{IN} = 4.2V, R_{LOAD} = 8Ω)

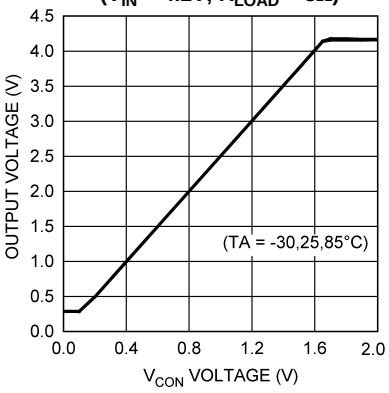


Figure 11.

Efficiency vs Output Voltage (V_{IN} = 3.9V)

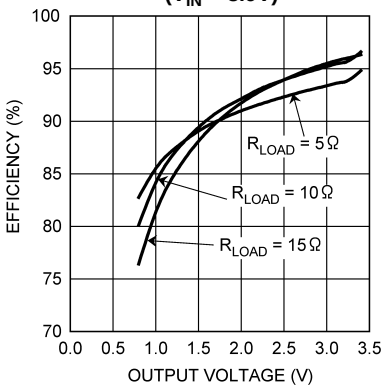


Figure 12.

Efficiency vs Output Current (V_{OUT} = 0.8V)

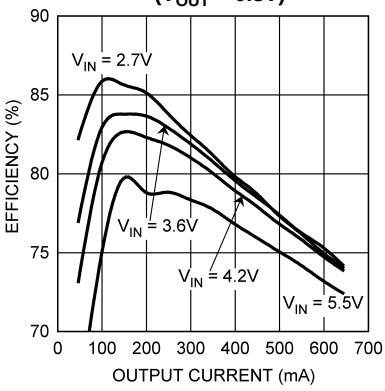


Figure 13.

Efficiency vs Output Current (V_{OUT} = 3.4V)

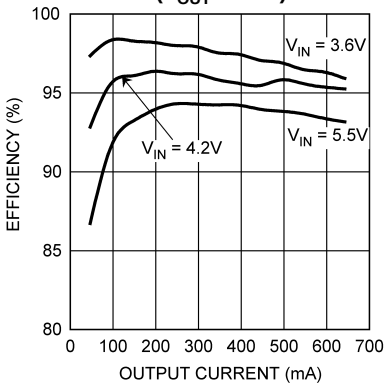


Figure 14.

Load Transient Response (V_{OUT} = 0.8V)

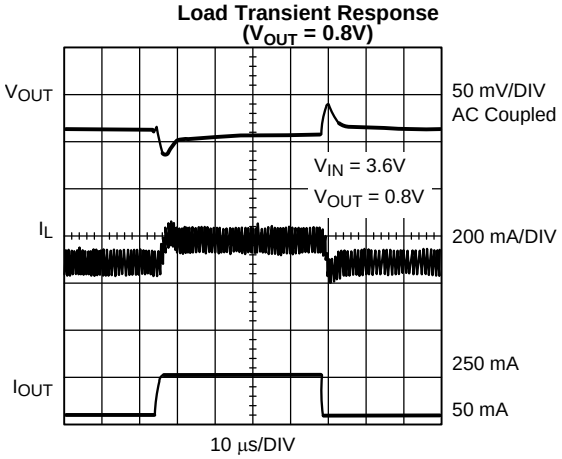


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, $PV_{IN} = V_{DD}$ = EN = 3.6V, L = 3.3uH, DCR of L ≤ 100mΩ, C_{IN} = 10uF, 0603, 6.3V (4.7uF||4.7uF, 0603, 6.3V can be used), C_{OUT} = 4.7uF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted)

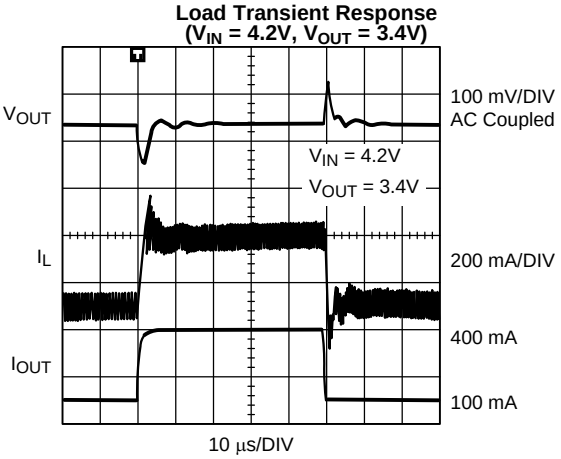


Figure 16.

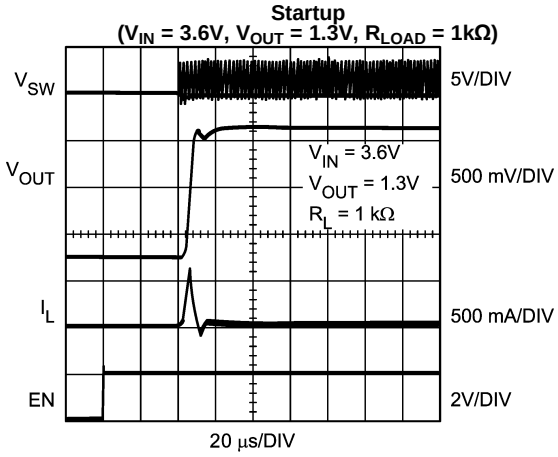


Figure 17.

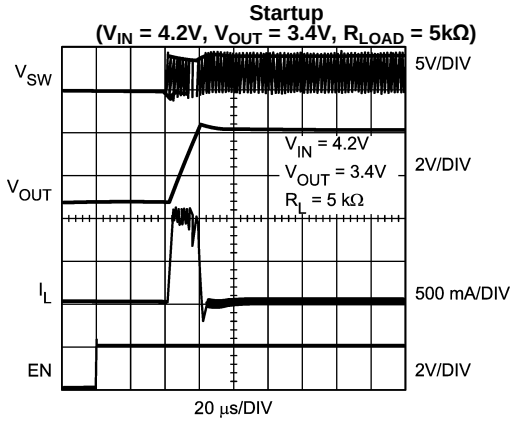


Figure 18.

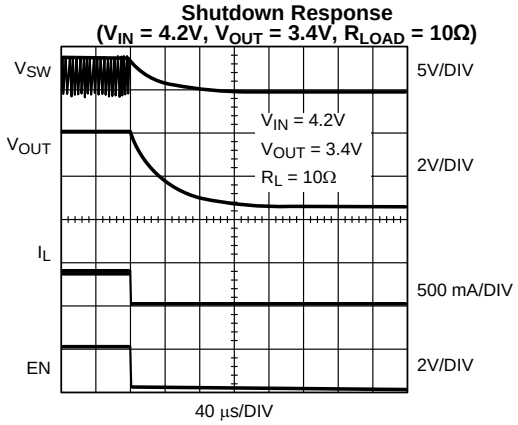


Figure 19.

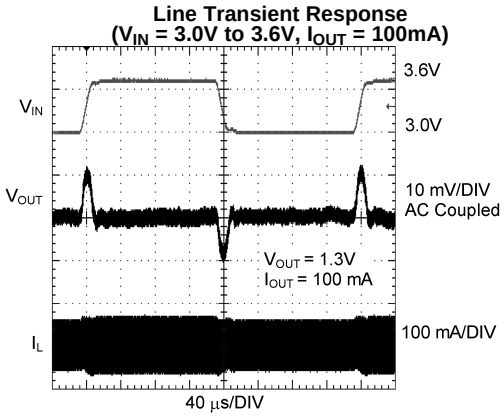


Figure 20.

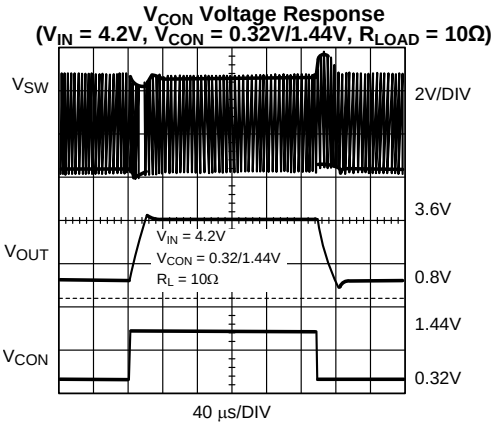


Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, $PV_{IN} = V_{DD} = EN = 3.6V$, L = 3.3uH, DCR of L ≤ 100mΩ, C_{IN} = 10uF, 0603, 6.3V (4.7uF||4.7uF, 0603, 6.3V can be used), C_{OUT} = 4.7uF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted)

V_{CON} and Load Transient
(V_{IN} = 4.2V, V_{CON} = 0.32V/1.44V, 15Ω/8Ω, same time)

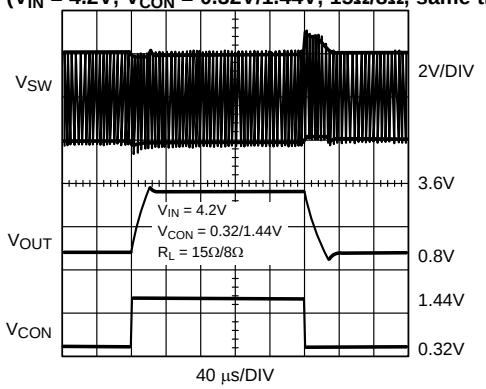


Figure 22.

Timed Current Limit Response
(V_{IN} = 3.6V)

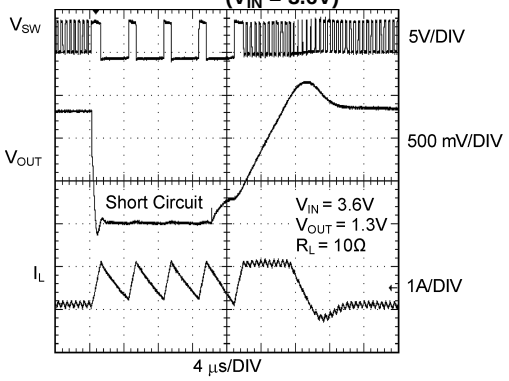


Figure 23.

Output Voltage Ripple
(V_{OUT} = 1.3V)

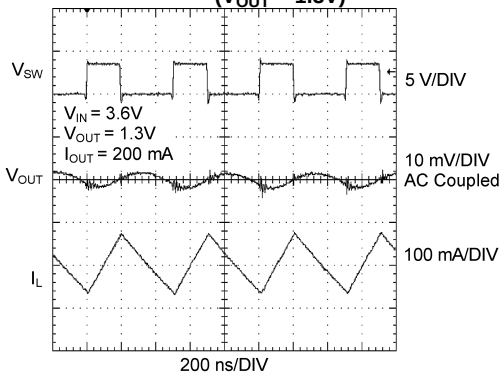


Figure 24.

Output Voltage Ripple
(V_{OUT} = 3.4V)

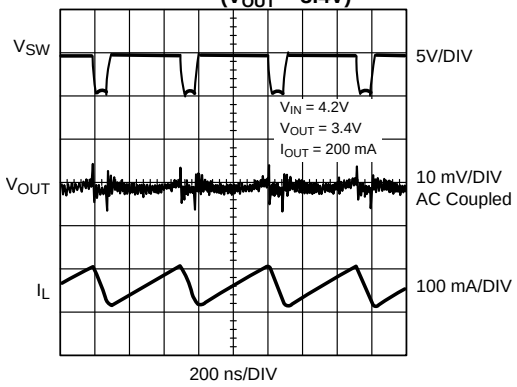


Figure 25.

Output Voltage Ripple in Pulse Skip
(V_{IN} = 3.64V, V_{OUT} = 3.4V, R_{LOAD} = 5Ω)

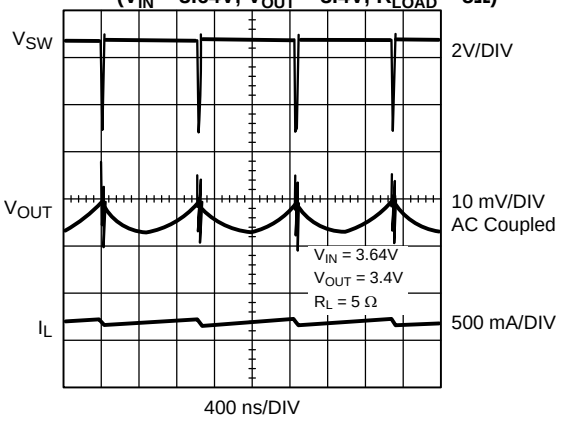


Figure 26.

R_{DSON} vs Temperature (DSBGA)
(P-ch, I_{SW} = 200mA)

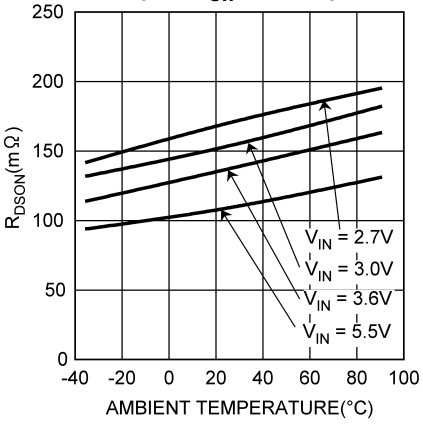


Figure 27.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, PV_{IN} = V_{DD} = EN = 3.6V, L = 3.3uH, DCR of L ≤ 100mΩ, C_{IN} = 10uF, 0603, 6.3V (4.7uF||4.7uF, 0603, 6.3V can be used), C_{OUT} = 4.7uF, 0603, 6.3V for LM3205TL/LM3205SD unless otherwise noted)

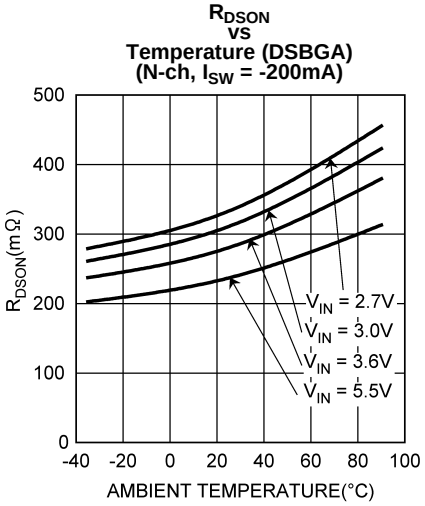


Figure 28.

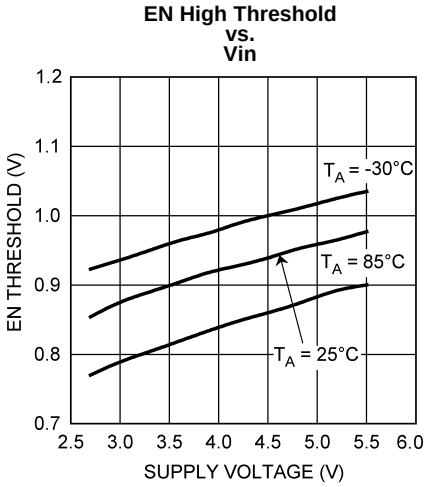


Figure 29.

BLOCK DIAGRAM

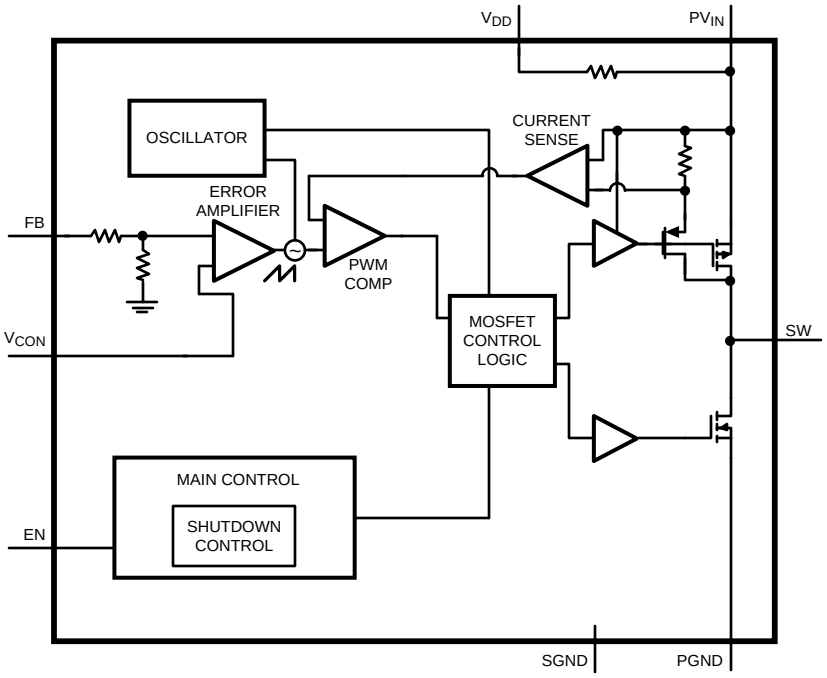


Figure 30. Functional Block Diagram

OPERATION DESCRIPTION

The LM3205 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a current-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 650mA in PWM mode.

Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

Efficiency is typically around 96% for a 400mA load with 3.4V output, 4.2V input. The output voltage is dynamically programmable from 0.8V (typ.) to 3.6V (typ.) by adjusting the voltage on the control pin without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3205 is constructed using a chip-scale 8-pin DSBGA or 10-pin WSON package. These packages offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (2MHz) reduces the size of external components. As shown in Figure 1, only three external power components are required for implementation. Use of a DSBGA package requires special design considerations for implementation. (See DSBGA Package Assembly and use in the Applications Information section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See Shutdown Mode in the Device Information section.)

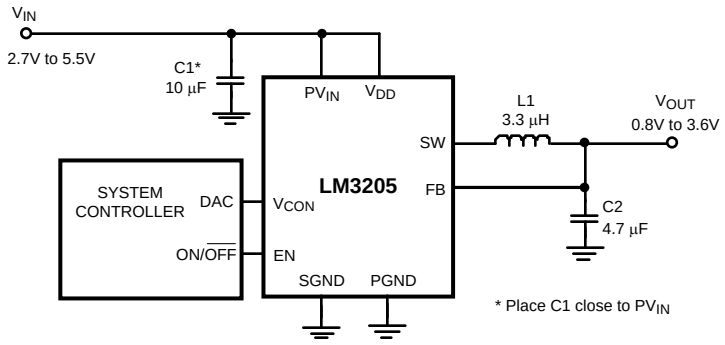


Figure 31. Typical Operating System Circuit

CIRCUIT OPERATION

Referring to Figure 1 and Figure 30, the LM3205 operates as follows. During the first part of each switching cycle, the control block in the LM3205 turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} - V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

While in operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load.

Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop. The minimum on time of PFET is 50ns (typ.)

SHUTDOWN MODE

Setting the EN digital pin low (<0.5V) places the LM3205 in a 0.01µA (typ.) Shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3205 are turned off. Setting EN high (>1.2V) enables normal operation.

EN should be set low to turn off the LM3205 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3205 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the LM3205 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across and ordinary rectifier diode.

With medium and heavy loads, the internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

CURRENT LIMITING

A current limit feature allows the LM3205 to protect itself and external components during overload conditions. In PWM mode, an 1200mA (max.) cycle-by-cycle current limit is normally used. If an excessive load pulls the output voltage down to approximately 0.375V, then the device switches to a timed current limit mode. In timed current limit mode the internal PFET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 3.5us to force the instantaneous inductor current to ramp down to a safe value. The synchronous rectifier is off in timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

The LM3205 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.8V(typ.) to 3.6V(typ.) by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See Setting the Output Voltage in the Application Information section for further details.

THERMAL OVERLOAD PROTECTION

The LM3205 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM3205 features a pin-controlled variable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.8V (typ.) to 3.6V (typ.) by setting the voltage on the V_{CON} pin, as in the following formula:

$$V_{OUT} = 2.5 \times V_{CON} \quad (1)$$

When V_{CON} is between 0.32V and 1.44V, the output voltage will follow proportionally by 2.5 times of V_{CON}.

If V_{CON} is over 1.44V (V_{OUT} = 3.6V), sub-harmonic oscillation may occur because of insufficient slope compensation. If V_{CON} voltage is less than 0.32V (V_{OUT} = 0.8V), the output voltage may not be regulated due to the required on-time being less than the minimum on-time (50ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to datasheet curve (V_{CON} Voltage vs Output Voltage) for details. This curve is for a typical part and there could be part-to-part variation for output voltages less than 0.8V over the limited V_{IN} range.

INDUCTOR SELECTION

A 3.3µH inductor with saturation current rating over 1200mA and low inductance drop at the full DC bias condition is recommended for almost all applications. The inductor's DC resistance should be less than 0.2Ω for good efficiency. For low dropout voltage, lower DCR inductors are advantageous. The lower limit of acceptable inductance is 2.3µH at 1200mA over the operating temperature range. Full attention should be paid to this limit, because some small inductors show large inductance drops at high DC bias. These can not be used with the LM3205. Taiyo-Yuden NR3015T3R3M is an example of an inductor with the lowest acceptable limit (as of Nov./05). Table 1 suggests some inductors and suppliers.

Table 1. Suggested inductors and their suppliers

Model	Size (WxLxH) [mm]	Vendor
NR3015T3R3M	3.0 x 3.0 x 1.5	Taiyo-Yuden
DO3314-332MXC	3.3 x 3.3 x 1.4	Coilcraft

If a smaller inductance inductor is used in the application, the LM3205 may become unstable during line and load transients and V_{CON} transient response times may get affected.

For low-cost applications, an unshielded bobbin inductor is suggested. For noise-critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can cause poor efficiency, regulation errors or stress to a DC-DC converter like the LM3205.

CAPACITOR SELECTION

The LM3205 is designed for use with ceramic capacitors for its input and output filters. Use a 10µF ceramic capacitor for input and a 4.7µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 2 lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. A few manufactures can supply 4.7µF capacitors in the 0805 case size which maintain at least 50% of their value, but TDK is currently the only manufacturer which can provide such capacitors in the 0603 case size. As of November, 2005, no manufacture can supply 10µF capacitors in the 0603 case size which maintain 50% of their value. If it is necessary to choose a 0603-size capacitor for V_{IN}, the operation of the LM3205 should be carefully evaluated on the system board. Output capacitors with smaller case sizes mitigate piezo electric vibrations when the output voltage is stepped up and down at fast rates. However, they have a larger percentage drop in value with dc bias. Use of multiple 2.2µF or 1µF capacitors in parallel may also be considered.

Table 2. Suggested capacitors and their suppliers

Model	Vendor
0805ZD475KA 4.7µF, 10V	AVX
C1608X5R0J475M, 4.7µF, 6.3V	TDK
C2012X5R0J106M,10µF, 6.3V	TDK

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3205 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

EN PIN CONTROL

Drive the EN pin using the system controller to turn the LM3205 ON and OFF. Use a comparator, Schmidt trigger or logic gate to drive the EN pin. Set EN high (>1.2V) for normal operation and low (<0.5V) for a 0.01µA (typ.) shutdown mode.

Set EN low to turn off the LM3205 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The part is out of regulation when the input voltage is less than 2.7V. The LM3205 is designed for mobile phones where the system controller controls operation mode for maximizing battery life and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in TI Application Note 1112 (SNVA009). Refer to the section *Surface Mount Technology (SMD) Assembly Considerations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 (SNVA009) for specific instructions how to do this.

The 8-Bump package used for LM3205 has 300micron solder balls and requires 10.82mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7mil wide, for a section approximately 7mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3205 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A3 and B3. Because PGND and PVIN are typically connected to large copper planes, inadequate thermal relief's can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

WSON PACKAGE ASSEMBLY AND USE

Use of the WSON package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in TI Application Note 1187 (SNOA401). Refer to the section *Surface Mount Technology (SMT) Assembly Recommendations.* For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device and must attach to the DAP(Die Attach Pad) of the WSON package. The pad style used with WSON package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1187 (SNOA401) for specific instructions how to do this.

BOARD LAYOUT CONSIDERATIONS

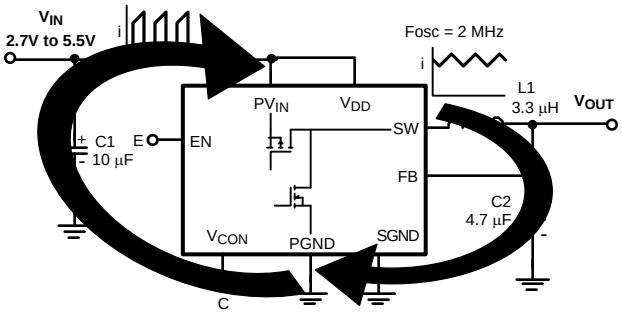


Figure 32. Current Loop

The LM3205 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from P_{VDD} line to the output capacitor (C2) through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2).

Referring to Figure 32 , the LM3205 has two major current loops where pulse and ripple current flow. The loop shown in the left hand side is most important, because pulse current shown in Figure 32 flows in this path. The right hand side is next. The current waveform in this path is triangular, as shown in Figure 32 . Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. Other lines, such as from battery to C1(+) and C2(+) to load, are almost DC current, so it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

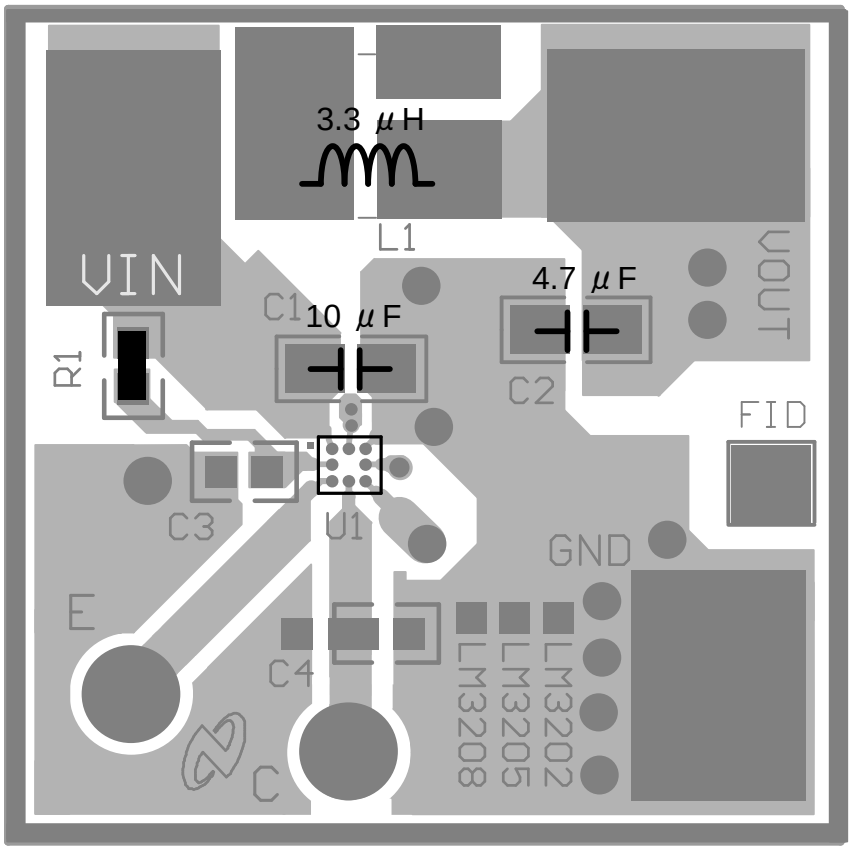


Figure 33. Evaluation Board Layout for DSBGA

BOARD LAYOUT FLOW (DSBGA)

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is most important.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. Above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C2(+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2(-) and PGND.)
6. V_{DD} should not be connected directly to PV_{IN}. Connecting these pins under the device should be avoided. It is good idea to connect V_{DD} to the C1(+) to avoid switching noise injection to the V_{DD} line.
7. FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.

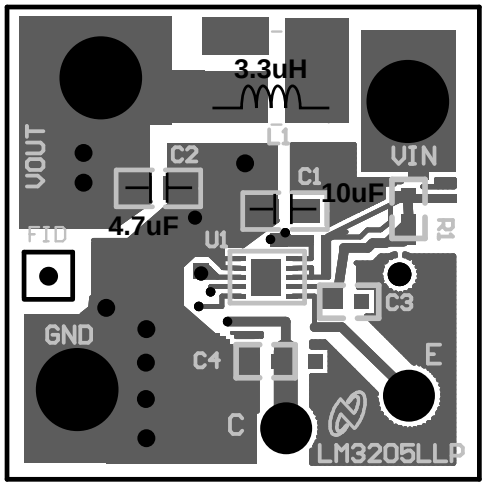


Figure 34. Evaluation Board for WSON

BOARD LAYOUT FLOW (WSON)

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is most important.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. Above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C2(+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should connect directly to PGND through a single common via as close to C1 as possible. Connecting these pins under the WSON device on a different layer should be avoided.
6. V_{DD} should not be connected directly to PV_{IN}. Connecting these pins under the device should be avoided. It is good idea to connect V_{DD} to the C1(+) to avoid switching noise injection to the V_{DD} line.
7. FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.

NOTE

The evaluation board shown in Figure 33 and Figure 34 for the LM3205TL/LM3205SD were designed with these considerations, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. The board can be used as a reference, but it is not the best. Please refer questions to a TI representative.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3205SD-2/NOPB	ACTIVE	WSON	DSC	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	S006B	Samples
LM3205TLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	S 32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

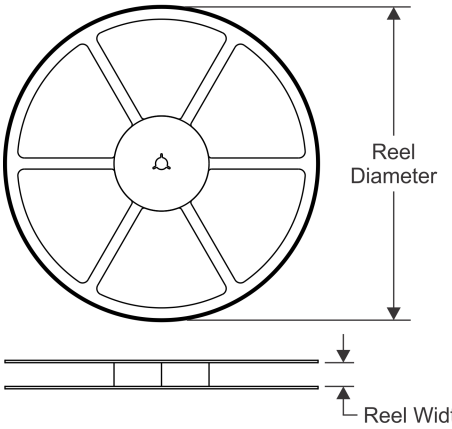
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

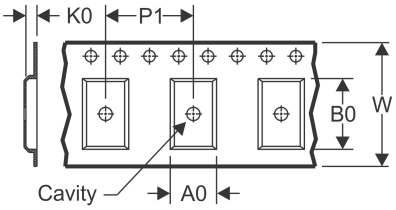
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

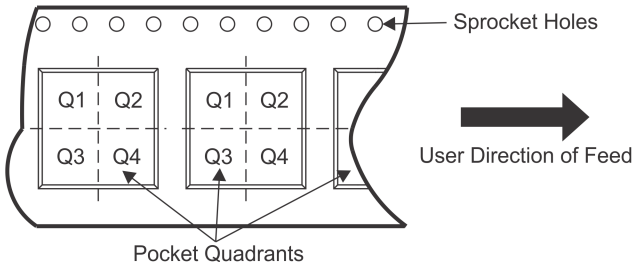


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

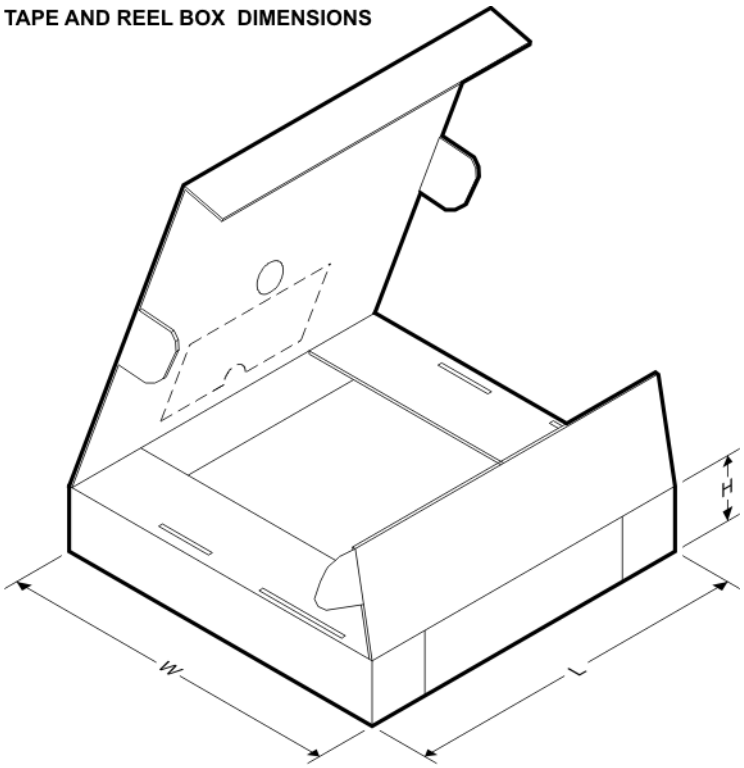
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3205SD-2/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM3205TLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

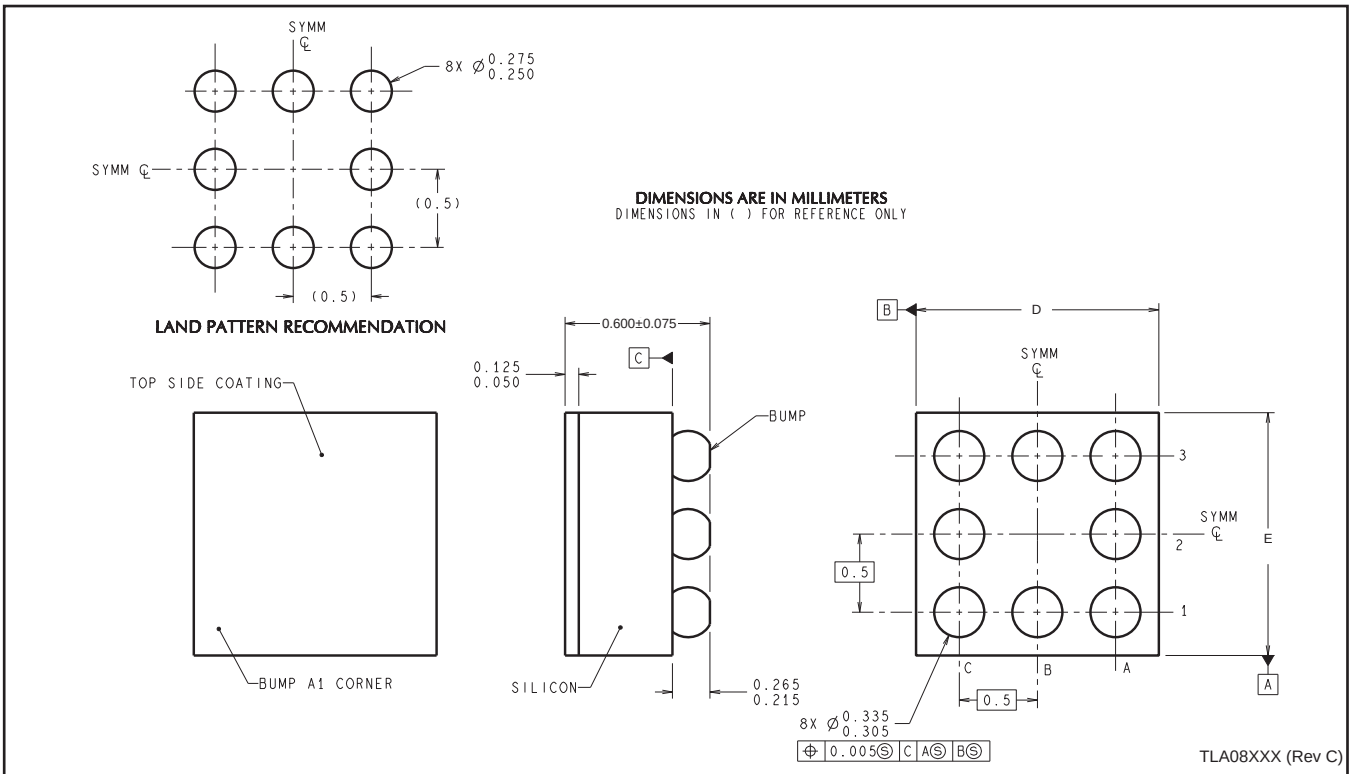
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3205SD-2/NOPB	WSON	DSC	10	1000	208.0	191.0	35.0
LM3205TLX/NOPB	DSBGA	YZR	8	3000	208.0	191.0	35.0

YZR0008



D: Max = 1.862 mm, Min =1.801 mm

E: Max = 1.713 mm, Min =1.652 mm

4215045/A 12/12

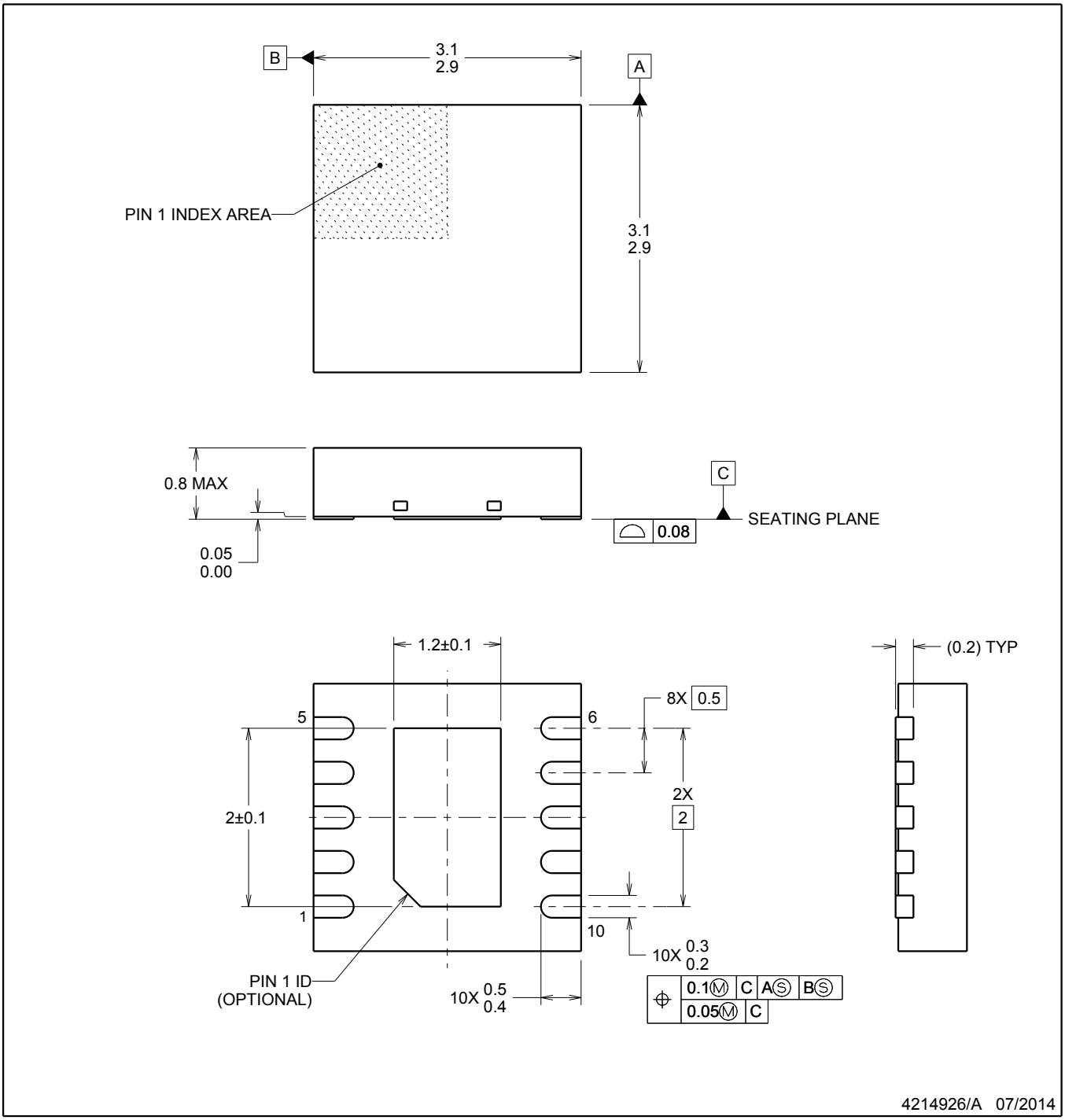
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

PACKAGE OUTLINE

DSC0010B

WSON - 0.8 mm max height

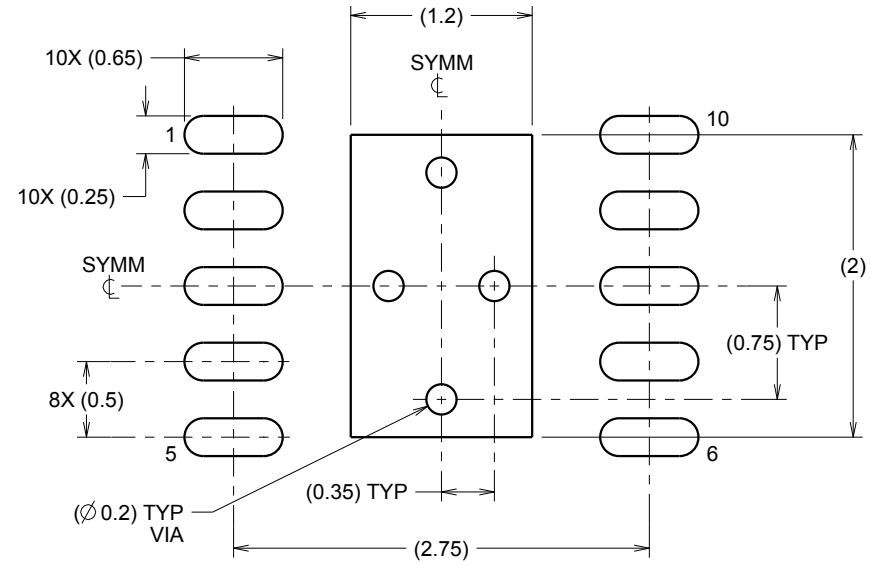
PLASTIC SMALL OUTLINE - NO LEAD



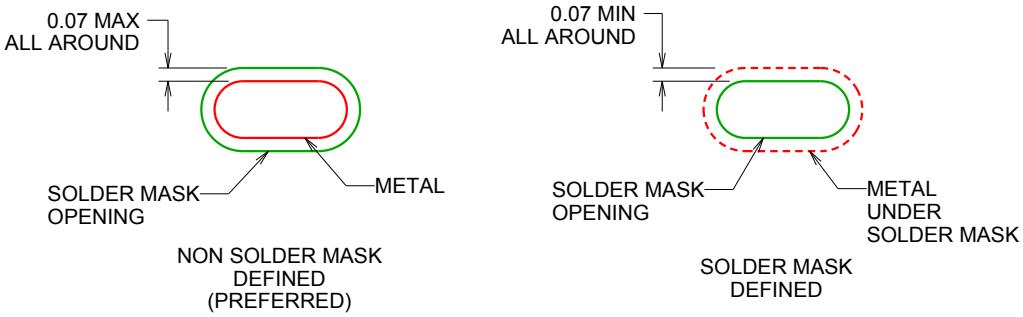
4214926/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

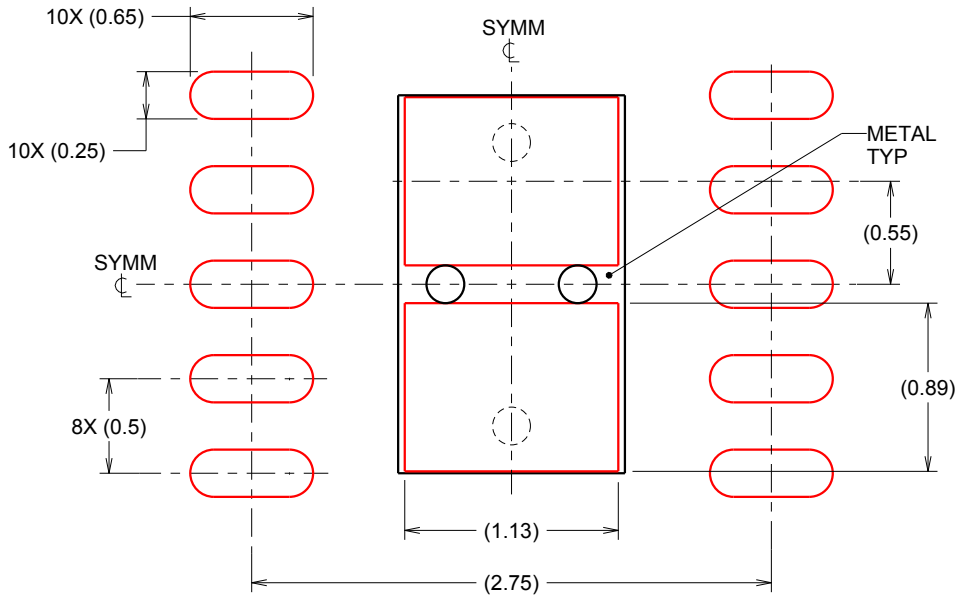
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSC0010B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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