2:1 MIPI D-PHY (2.5 Gbps) 4-Data Lane & C-PHY (2.5 Gsps) 3-Data Lane Switch

Description

The FSA646 is a four-data-lane D-PHY or three-data-lane C-PHY, MIPI switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The FSA646 is designed for the MIPI specification and allows connection to a SCI or DSI module.

Features

- Switch Type: SPDT (10x)
- Signal Types:
 - MIPI, D-PHY & C-PHY
- V_{CC}: 1.5 to 5.0 V
- Input Signals: 0 to 1.3 V
- R_{ON}:
 - 6 Ω Typical HS MIPI
 - 6 Ω Typical LP MIPI
- ΔR_{ON} : 0.1 Ω Typical LP & HS MIPI
- $\Delta R_{ON\ FLAT}$: 0.9 Ω Typical LP & HS MIPI
- I_{CCZ}: 1 μA Maximum
- I_{CC}: 32 μA Typical
- O_{IRR}: -24 dB Typical
- Bandwidth: 4.1 GHz Typical
- Xtalk: -30 dB Typical
- C_{ON}: 1.5 pF Typical
- Skew (P), Skew (O): 6 ps Typical
- This is a Pb-Free Device

Applications

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays



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(Bottom View)

WLCSP36, 2.43x2.43x0.4 CASE 567WJ

MARKING DIAGRAM

GSKK XYZ

GS = Specific Device Code

KK = Assembly Lot

X = Year

Y = Work Week

Z = Assembly Location

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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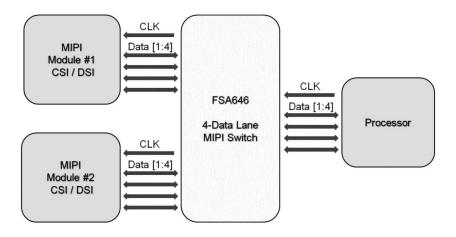


Figure 1. Typical D-PHY Application

PIN DESCRIPTIONS

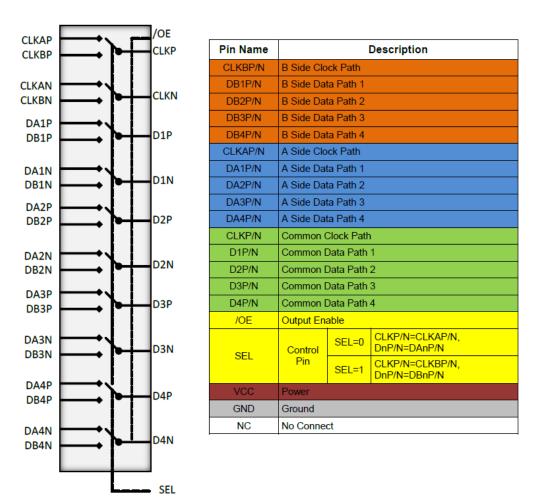


Figure 2. Analog Symbol

PIN DEFINITIONS

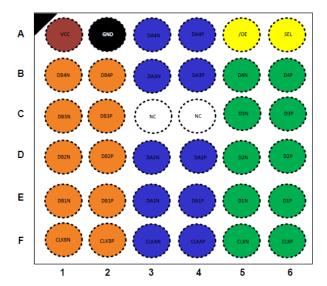


Figure 3. Top Through View

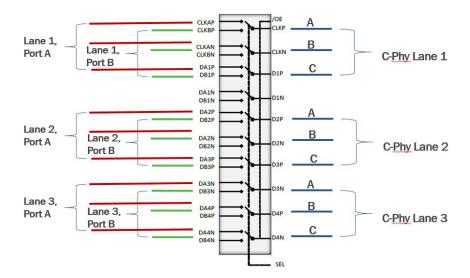


Figure 4. Recommended C-PHY Configuration

Table 1. BALL-TO-PIN MAPPINGS

| Ball | Pin Name | Ball | Pin Name | Ball | Pin Name |
|------|-----------------|------|----------|------|----------|
| A1 | V _{CC} | C1 | DB3N | E1 | DB1N |
| A2 | GND | C2 | DB3P | E2 | DB1P |
| A3 | DA4N | C3 | NC | E3 | DA1N |
| A4 | DA4P | C4 | NC | E4 | DA1P |
| A5 | /OE | C5 | D3N | E5 | D1N |
| A6 | SEL | C6 | D3P | E6 | D1P |
| B1 | DB4N | D1 | DB2N | F1 | CLKBN |
| B2 | DB4P | D2 | DB2P | F2 | CLKBP |
| В3 | DA3N | D3 | DA2N | F3 | CLKAN |
| B4 | DA3P | D4 | DA2P | F4 | CLKAP |
| B5 | D4N | D5 | D2N | F5 | CLKN |
| B6 | D4P | D6 | D2P | F6 | CLKP |

TRUTH TABLE

| SEL | /OE | Function |
|---------|------|--|
| LOW LOW | | $CLK_P = CLKA_P$, $CLK_N = CLKA_N$, $Dn(P/N) = DAn(P/N)$ |
| HIGH | LOW | $CLK_P = CLKB_P$, $CLK_N = CLKB_N$, $Dn(P/N) = DBn(P/N)$ |
| X | HIGH | Clock and Data Ports High Impedance |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | | Max. | Unit |
|--------------------|--|------------------------|------|-----------------|------|
| V _{CC} | Supply Voltage | | -0.5 | 6.0 | V |
| V _{CNTRL} | DC Input Voltage (/OE, SEL) | (Note 1) | -0.5 | V _{CC} | V |
| V _{SW} | DC Switch I/O Voltage | (Note 1,2) | -0.3 | 1.8 | V |
| I _{IK} | DC Input Diode Current | DC Input Diode Current | | | mA |
| l _{OUT} | DC Output Current | | | 25 | mA |
| T _{STG} | Storage Temperature | | -65 | +150 | °C |
| ESD | Human Body Model, JEDEC: JESD22-A114 | All Pins | 2.0 | | kV |
| | Charged Device Model, JEDEC: JESD22-C101 | | | | |
| | IEC 61000-4-2 System Contact | | 8.0 | | |
| | | Air Gap | 15.0 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Parameter | | | Unit |
|--------------------|---|---|-----|-----------------|------|
| V _{CC} | Supply Voltage | | 1.5 | 5.0 | V |
| V _{CNTRL} | Control Input Voltage (SEL, /OE) | Control Input Voltage (SEL, /OE) (Note 3) | | V _{CC} | V |
| V _{SW} | - · · · · · · · · · · · · · · · · · · · | -HS Mode | 0 | 0.3 | V |
| | (CLKn, Dn, CLKAn, CLKBn, Dan, DBn) | -LS Mode | 0 | 1.3 | V |
| T _A | Operating Temperature | | -40 | +85 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must no float.

The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
 V_{SW} refers to analog data switch paths.

$\textbf{DC AND TRANSIENT CHARACTERISTICS} \ (T_{A} = 25^{\circ}C \ unless \ otherwise \ specified)$

| | | | | T _A = | -40 to +8 | B5°C | |
|--|---|--|---------------------|------------------|-----------|------|------|
| Symbol | Parameter | Conditions | V _{CC} (V) | Min. | Тур. | Max. | Unit |
| V _{IK} | Clamp Diode Voltage (/OE, SEL) | I _{IN} = -18 mA | 1.5 | -1.2 | | -0.6 | V |
| V _{IH} | Input Voltage High | SEL, /OE | 1.5 to 5 | 1.3 | | | V |
| V _{IL} | Input Voltage Low | SEL, /OE | 1.5 to 5 | | | 0.5 | V |
| I _{IN} | Control Input Leakage (/OE, SEL) | V _{CNTRL} = 0 to V _{CC} | 5 | -0.5 | | 0.5 | μΑ |
| I _{NO(OFF)} I _{NC(OFF)} | Off Leakage Current of Port CLKAn, Dan, CLKBn and DBn | V _{SW} = 0.0 ≤ DATA ≤ 1.3 V | 5 | -0.5 | | 0.5 | μΑ |
| I _{A(ON)} | ON Leakage Current of Common Ports (CLKn, Dn) | V _{SW} = 0.0 ≤ DATA ≤ 1.3 V | 5 | -0.5 | | 0.5 | μА |
| I _{OFF} | Power-Off Leakage Current (All I/O Ports) | V _{SW} = 0.0 or 1.3 V | 0 | -0.5 | | 0.5 | μΑ |
| l _{OZ} | Off-State Leakage | $V_{SW} = 0.0 \le DATA \le 1.3 \text{ V}$ /OE = High | 5 | -0.5 | | 0.5 | μΑ |
| R _{ON_MIPI_HS} | Switch On Resistance for | I _{ON} = -8 mA, /OE = 0 V, | 1.5 | | 6 | | Ω |
| | HS MIPI Applications (Note 4) | SEL = V_{CC} or 0 V, CLKA, CLKB, DB _N or DA _N = 0.2 V | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| R _{ON_MIPI_LP} | Switch On Resistance for | I _{ON} = -8 mA, /OE = 0 V, | 1.5 | | 6 | | Ω |
| | LP MIPI Applications (Note 4) | OLIND, DDN OF DAN = 1.2 V | 2.5 | | | | |
| | | | 3.3 | | | | |
| | | | 5 | | | | |
| $\Delta R_{ON_MIPI_HS}$ | On Resistance Matching Between HS MIPI | I _{ON} = -8 mA, /OE = 0 V, SEL = V _{CC} or 0 V, CLKA, | 1.5 | | 0.1 | | Ω |
| | Channels | CLKB, DB_N or $DA_N = 0.2 \text{ V}$ | 2.5 | | | | |
| | (Note 4) | | 3.3 | | | | |
| | | | 5 | | | | |
| $\Delta R_{ON_MIPI_LP}$ | On Resistance Matching Between LP MIPI | $I_{ON} = -8$ mA, $/OE = 0$ V, SEL = V_{CC} or 0 V, CLKA, | 1.5 | | 0.1 | | Ω |
| | Channels | CLKB, DB _N or DA _N = 1.2 V | 2.5 | | | | |
| | (Note 4) | | 3.3 | | | | |
| | | | 5 | | | | |
| R _{ON_FLAT_MIPI_HS} | On Resistance Flatness for HS MIPI Signals | I _{ON} = -8 mA, /OE = 0 V, | 1.5 | | 0.9 | | Ω |
| | (Note 4) | SEL = V_{CC} or 0 V, CLKA, CLKB, DB _N or DA _N = 0 to | 2.5 | | | | |
| | | 0.3 V | 3.3 | | | | |
| | | | 5 | | | | |
| R _{ON_FLAT_MIPI_LP} | On Resistance Flatness for LP MIPI Signals | I _{ON} = -8 mA, /OE = 0 V, | 1.5 | | 0.9 | | Ω |
| | (Note 4) | SEL = V_{CC} or 0 V, CLKA, CLKB, DB _N or DA _N = 0 to | 2.5 | | | | |
| | | 1.3 V | 3.3 | | | | |
| | | | 5 | | | | |
| I _{CC} | Quiescent Supply Current (Includes Change Pump) | V _{SEL} = 0 or V _{CC} , I _{OUT} = 0, /OE = 0 V | 5 | | | 30 | μΑ |

$\textbf{DC AND TRANSIENT CHARACTERISTICS} \ (T_A = 25^{\circ}C \ unless \ otherwise \ specified) \ (continued)$

| | | | | T _A = | -40 to +8 | 35°C | |
|------------------|---|--|---------------------|------------------|-----------|------|------|
| Symbol | Parameter | Conditions | V _{CC} (V) | Min. | Тур. | Max. | Unit |
| I _{CCZ} | Quiescent Supply Current (High Impedance) | V _{SEL} = 0 or V _{CC} , I _{OUT} = 0, /OE = 0 V | 5 | | | 1 | μΑ |
| Ісст | Increase in I _{CC} Current Per Control Voltage and V _{CC} | $V_{SEL} = 0$ or V_{CC} , $/OE = 1.5 V$ | 5 | | 1 | | μΑ |

^{4.} Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

AC ELECTRICAL CHARACTERISTICS (V $_{CC}$ = 3.3 V and T $_{A}$ = 25 $^{\circ}C$ unless otherwise specified)

| | | | | $T_A = -40 \text{ to } +85^{\circ}\text{C}$ | | | |
|-------------------|--|--|---------------------|---|------|------|------|
| Symbol | Parameter | Conditions | V _{CC} (V) | Min. | Тур. | Max. | Unit |
| [†] INIT | Initialization Time V _{CC} to Output (Note 5) | $\begin{aligned} R_L &= 50 \ \Omega, \ C_L = 0 \ pF, \\ V_{SW} &= 0.6 \ V \end{aligned}$ | 1.5 to 5 | | 60 | | μs |
| t _{EN} | Enable Time /OE to Output | $\begin{aligned} R_L &= 50~\Omega, C_L = 0~\text{pF}, \\ V_{SW} &= 0.6~\text{V} \end{aligned}$ | 1.5 to 5 | | 60 | 150 | μs |
| t _{DIS} | Disable Time /OE to Output | $\begin{aligned} R_L &= 50 \ \Omega, \ C_L = 0 \ \text{pF}, \\ V_{SW} &= 0.6 \ \text{V} \end{aligned}$ | 1.5 to 5 | | 35 | 250 | ns |
| t _{ON} | Turn-On Time SEL to Output | $R_L = 50 \Omega, C_L = 0 pF, V_{SW} = 0.6 V$ | 1.5 to 5 | | 350 | 1100 | ns |
| t _{OFF} | Turn-Off Time SEL to Output | $\begin{aligned} R_L &= 50 \ \Omega, \ C_L = 0 \ \text{pF}, \\ V_{SW} &= 0.6 \ \text{V} \end{aligned}$ | 1.5 to 5 | | 125 | 800 | ns |
| t _{BBM} | Break-Before-Make Time | $R_L = 50 \Omega, C_L = 0 pF, V_{SW} = 0.6 V$ | 1.5 to 5 | 50 | | 450 | ns |
| t _{PD} | Propagation Delay (Note 5) | C_L = 0 pF, R_L = 50 Ω | 1.5 to 5 | 30 | 67 | 100 | ps |
| O _{IRR} | Off Isolation for MIPI (Note 5) | R_L = 50 Ω , f = 1250 MHz, /OE = HIGH, V_{SW} = 0.2 V_{PP} | 1.5 to 5 | | -24 | | dB |
| X _{TALK} | Crosstalk for MIPI (Note 5) | R_L = 50 Ω , f = 1250 MHz, SEL = High, V_{SW} = 0.2 V_{PP} | 1.5 to 5 | | -30 | -25 | dB |
| | | $R_L = 50 \Omega$, $f = 1250 MHz$, SEL = Low, $V_{SW} = 0.2 V_{PP}$ | | | -30 | -25 | |
| BW | -3 db Bandwidth (Note 5) | $\begin{aligned} R_L &= 50 \ \Omega, \ C_L = 0 \ \text{pF}, \\ V_{SW} &= 0.2 \ V_{PP} \end{aligned}$ | 1.5 to 5 | 2.5 | 4.1 | | GHz |
| IL | Insertion Loss at 750 MHz (Note 5) | $\begin{aligned} R_L &= 50~\Omega, C_L = 0~\text{pF}, \\ V_{SW} &= 0.2~\text{V}_{PP} \end{aligned}$ | 1.5 to 5 | | -0.7 | | dB |

^{5.} Guaranteed by characterization.

HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

| | | | | T _A = | A = -40 to +85°C | | | |
|--------------------|--|--|---------------------|------------------|------------------|------|------|--|
| Symbol | Parameter | Conditions | V _{CC} (V) | Min. | Тур. | Max. | Unit | |
| t _{SK(P)} | HS Mode Skew of Opposite Transitions of the Same Output (Note 6) | $\begin{aligned} R_L &= 50 \ \Omega, \ C_L = 0 \ pF, \\ V_{SW} &= 0.3 \ V \end{aligned}$ | 1.5 to 5 | | 6 | | ps | |
| t _{SK(O)} | HS Mode Skew of Channel-to-Channel Single-Ended Skew (Note 6) | R_L = 50 Ω , C_L = 0 pF, V_{SW} = 0.3 V | 1.5 to 5 | | 6 | | ps | |

^{6.} Guaranteed by characterization.

CAPACITANCE

| | | | T _A = -40 to +85°C | | | |
|------------------|---|---|-------------------------------|------|------|------|
| Symbol | Parameter | Conditions | Min. | Тур. | Max. | Unit |
| C _{IN} | Control Pin Input Capacitance (Note 7) | V _{CC} = 0 V, f = 1 MHz | | 2.1 | | pF |
| C _{ON} | On Capacitance (Note 7) | V_{CC} = 3.3 V, /OE = 0 V, f = 1250 MHz (in HS common value) | | 1.5 | | |
| C _{OFF} | On Capacitance (Note 7) | V _{CC} and /OE = 3.3 V, f = 1250 MHz (both sides in HS common value) | | 0.9 | | |

^{7.} Guaranteed by characterization.

The table below pertains to the Packaging information on the following page.

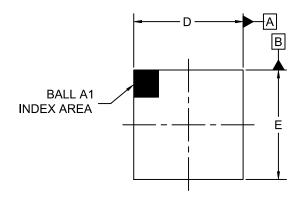
ORDERING INFORMATION

| Part Number | Top Marking | Package | Top Mark |
|-------------|--------------|---|----------|
| FSA646UCX | −40 to +85°C | 36-Ball WLCSP, Non-JEDEC 2.43 x 2.43 mm, 0.4 mm Pitch | GS |

ON

WLCSP36 2.43x2.43x0.488 CASE 567WJ ISSUE A

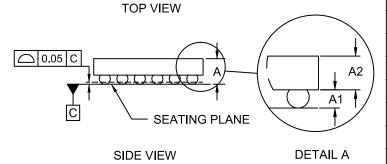
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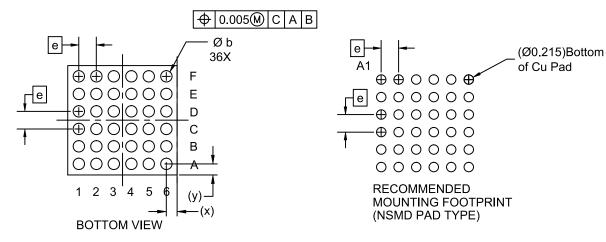


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

| | MILLIMETERS | | | | | |
|-----|-------------|----------|-------|--|--|--|
| DIM | MIN. | NOM. | MAX. | | | |
| Α | 0.450 | 0.488 | 0.526 | | | |
| A1 | 0.176 | 0.196 | 0.216 | | | |
| A2 | 0.274 | 0.292 | 0.310 | | | |
| b | 0.240 | 0.260 | 0.280 | | | |
| D | 2.400 | 2.430 | 2.460 | | | |
| E | 2.400 | 2.430 | 2.460 | | | |
| е | | 0.40 BSC | | | | |
| х | 0.200 | 0.215 | 0.230 | | | |
| у | 0.200 | 0.215 | 0.230 | | | |





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