Active Errata List

- UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection
- During UART Reception, Clearing REN May Generate Unexpected IT
- JBC/Double IT When External IT Occurs During JBC Instruction
- Timer2/Downcounter Mode/Double IT With Slow External Clock
- Input Trigger Consumption/All C51 Type I/O Ports
- MOVX/Port0/Read Mode

Errata History

AT80C51RA2

Lot Number	Errata List
All	T02,T03,T04,T05,T06

TS80C51RB2

Lot Number	Errata List
≤ 38584	T01, T02 ,T03, T04, T05, T06
> 38584	T02 ,T03, T04, T05, T06

TS87C51RB2

Lot Number	Errata List
≤ 36425	T01, T02 ,T03, T04, T05, T06
> 36425	T02 ,T03, T04, T05, T06

Errata Descriptions

1. UART/Reception in Modes 1, 2 and 3/UART False Start Bits Detection

When a false start bit occurs on the UART, some UART internal signals are not reset. Then when a real start bit occurs, the sampling is shifted.

Workaround

None.

2. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is clear between a start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of Interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

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Errata Sheet

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3. JBC/Double IT When External IT Occurs During JBC Instruction

On polling algorithm in ISR on IE1 or IE0, when the external IT appears during JBC instruction, the flag is not cleared. On the next JBC instruction another IT is pending. Therefore, the same IT is seen twice.

Workaround

Use JB Instruction instead of JBC instruction to test bit and CLR instruction to clear it.n twice.

4. Timer2/Downcounter Mode/Double IT with Slow External Clock

Double IT with slow external clock in downcount mode. Timer 2 in 16-bit autoreload in count-down mode with external clock input two interrupts are generated successively with low frequency on clock input (typ 10-40 KHz).

Workaround

Reload FFFE into TH2-TL2 in ISR and count down to RCAP-1 (to recover cycle lost in ISR)

Caution: do not work if initially RCAP = 0x0000

5. Input Trigger Consumption/All C51 Type I/O Ports

Some static consumption in input triggers of I/O ports may occur when entries are driven close to the trigger threshold (1 mA to 2 mA for each I/O at Vin = 2.4V for Vcc = 5V)

Workaround

None.

6. Movx/Port0/Read Mode

When reading External Ram using Movx instruction, Port0's SFR may contain '0' whereas any acces to external memories (data or program) should write '1' into them .

'0' is written to each bit of the Port0 buffers prior to a Movx access. This problem has no consequence when the Movx cycle is a write, as the correct value is immediately substitued and is present on Port0 during the duration of the write pulse ($\overline{WR}$ = 0). When the Movx is a read, the strong internal pull-down N transistor creates a short circuit with the external RAM buffer or peripheral when the RAM or peripheral reads '1'.

Workaround

Replace any movx A,@Ri instruction by the sequence:

```
mov P0, #FFh
movx A, @Ri
```

Replace any movx A,@DPTR instruction by the sequence:

```
mov P0, #FFh
movx A, @DPTR
```

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