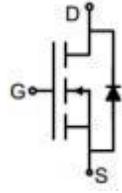
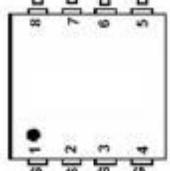
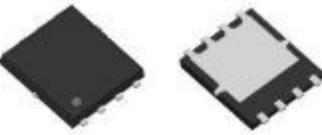


N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The G50N03D5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} 30V ● I_D (at $V_{GS} = 10V$) 50A ● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 4.5mΩ ● $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 8mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	 <p>Schematic diagram</p>  <p>Marking and pin assignment</p>  <p>DFN5*6-8L</p>		
Device	Package	Marking	Packaging
G50N03D5	DFN5*6-8L	G50N03	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Continuous Drain Current	I_D	50	A
Pulsed Drain Current (note1)	I_{DM}	200	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	20	W
Single pulse avalanche energy (note2)	E_{AS}	81	mJ
Operating Junction and Storage Temperature Range	T_J, T_{Stg}	-55 To 150	$^\circ\text{C}$
Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	78	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	R_{thJC}	6	$^\circ\text{C}/\text{W}$

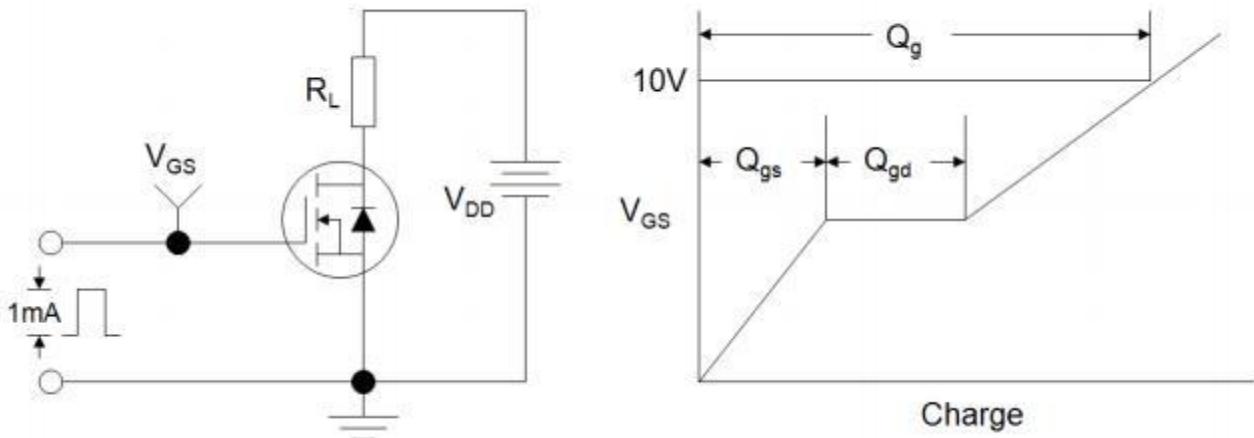
Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.1	1.6	2.4	V
Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$	--	3.2	4.5	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$	--	5.9	8	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 5\text{V}, I_D = 20\text{A}$	--	35	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1.0\text{MHz}$	--	1661	--	pF
Output Capacitance	C_{oss}		--	338	--	
Reverse Transfer Capacitance	C_{rss}		--	316	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = 15\text{V}, I_D = 20\text{A}, V_{\text{GS}} = 10\text{V}$	--	38.4	--	nC
Gate-Source Charge	Q_{gs}		--	5.8	--	
Gate-Drain Charge	Q_{gd}		--	7.9	--	
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 5\text{V}, I_D = 20\text{A}, R_G = 6\Omega$	--	7	--	ns
Turn-on Rise Time	t_r		--	6	--	
Turn-off Delay Time	$t_{\text{d(off)}}$		--	30	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_s	$T_c = 25^\circ\text{C}$	--	--	50	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 20\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 20\text{A}, V_{\text{GS}} = 0\text{V}$ $di/dt = 500\text{A}/\mu\text{s}$	--	57	--	nC
Reverse Recovery Time	T_{rr}		--	21	--	ns

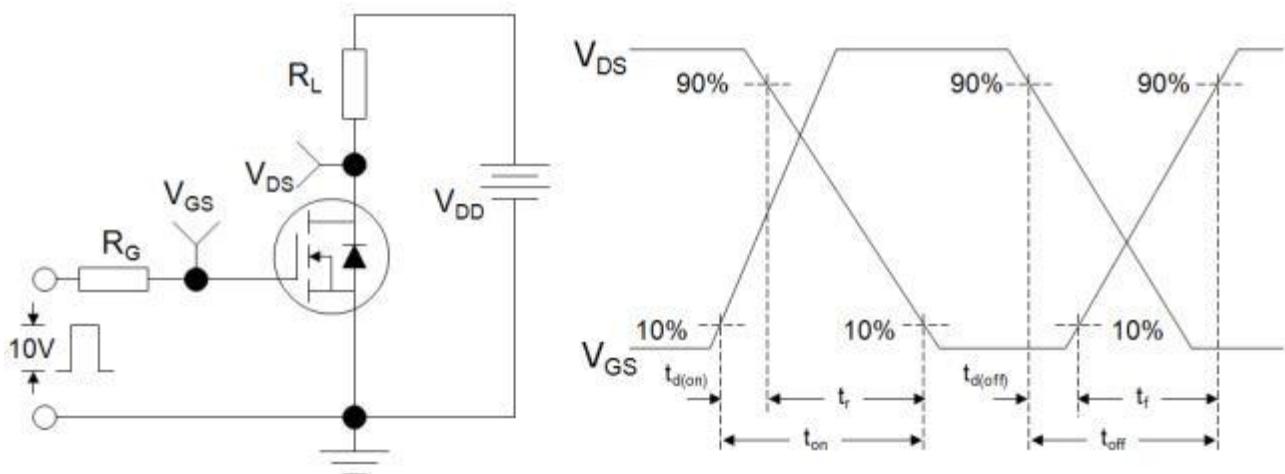
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

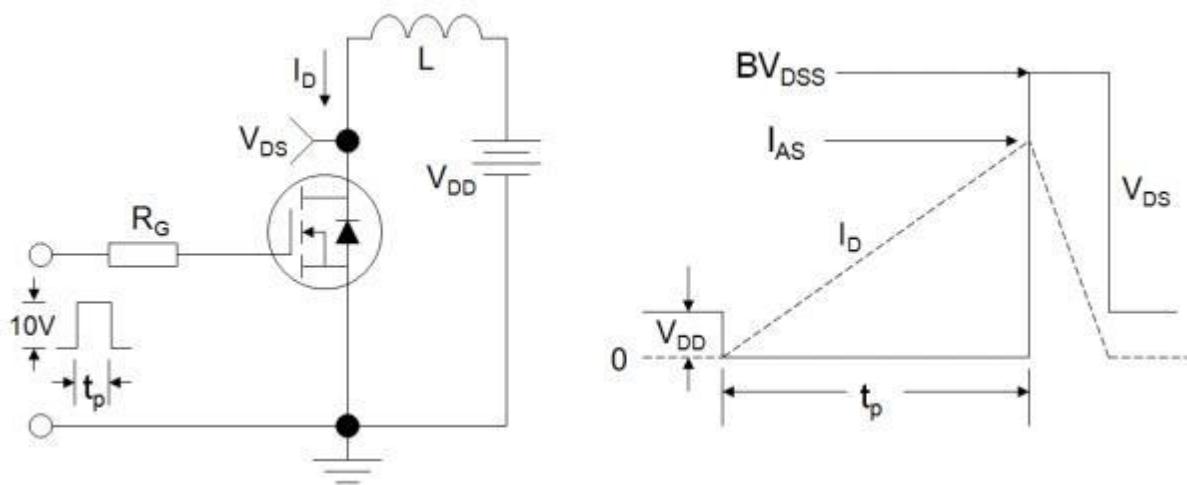
Gate Charge Test Circuit



Switch TimeTest Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

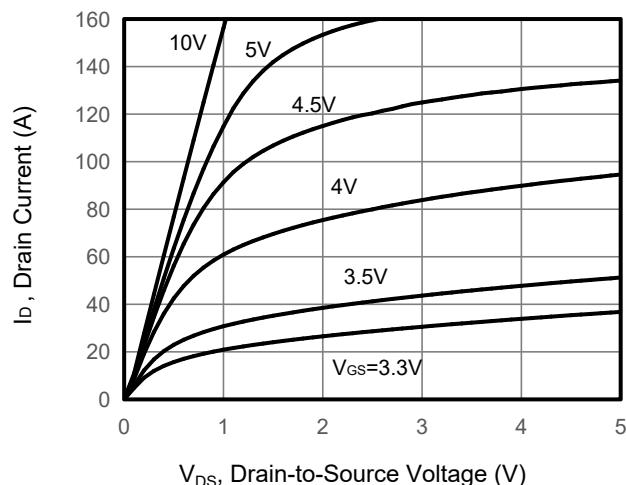


Figure 2. Transfer Characteristics

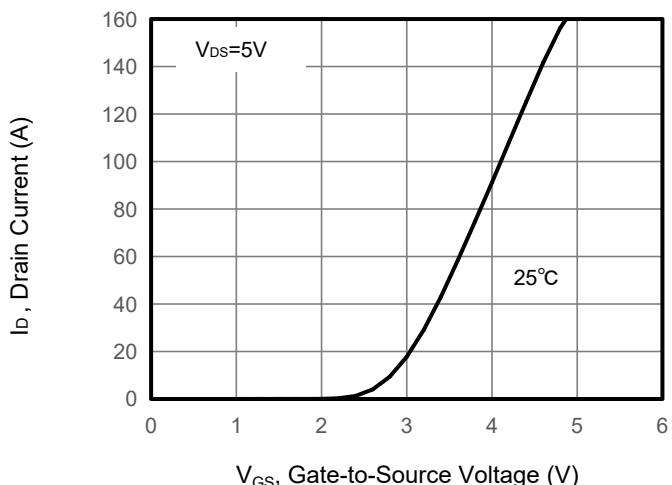


Figure 3. Drain Source On Resistance

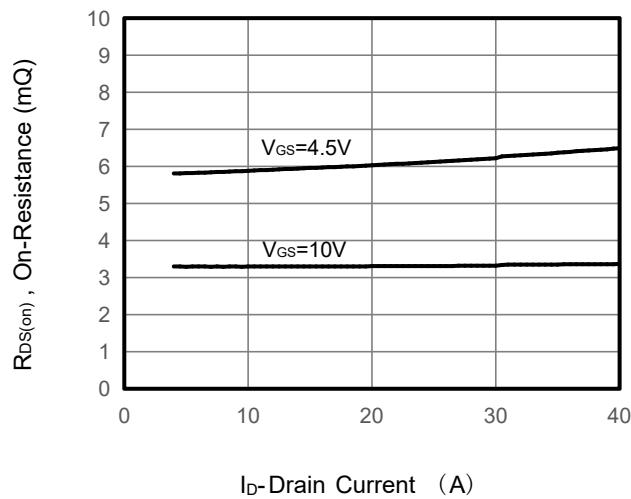


Figure 4. Gate Charge

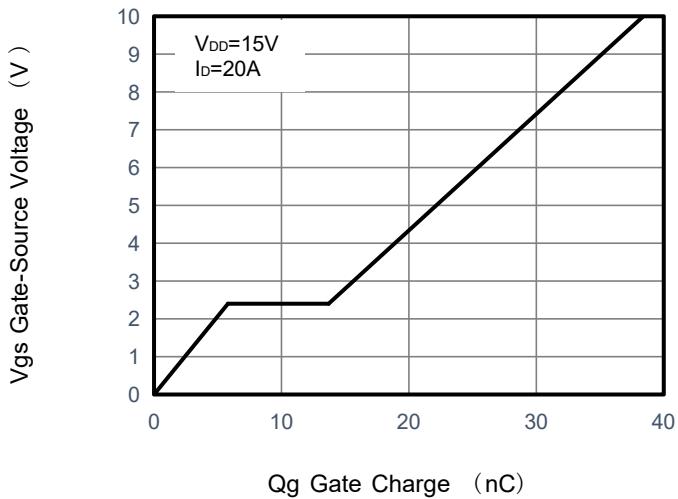


Figure 5 . Capacitance

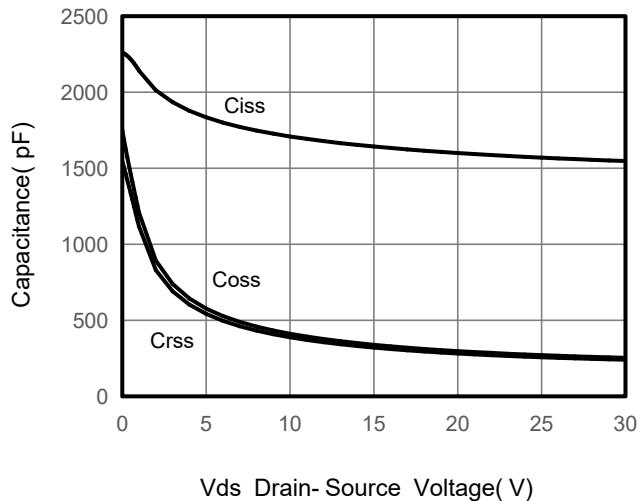
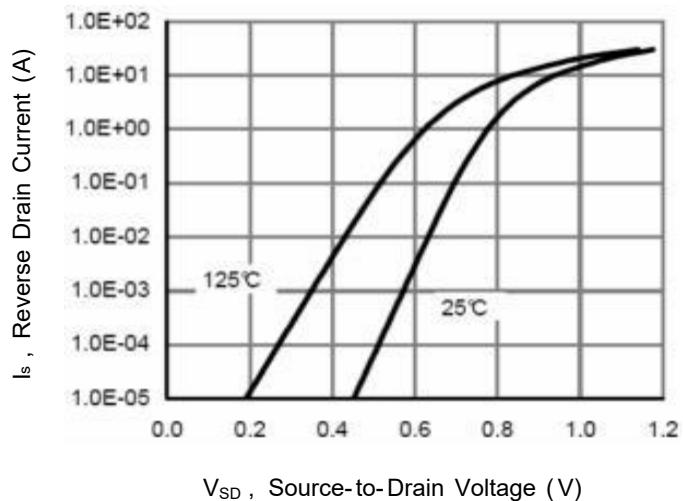


Figure 6 . Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7 . Drain- Source On- Resistance

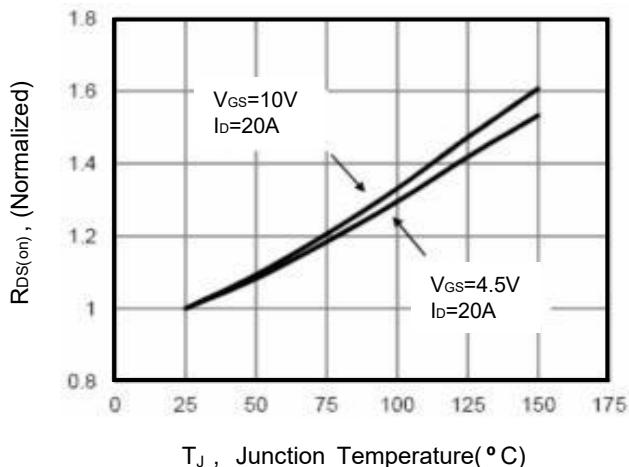


Figure 8. Safe Operation Area

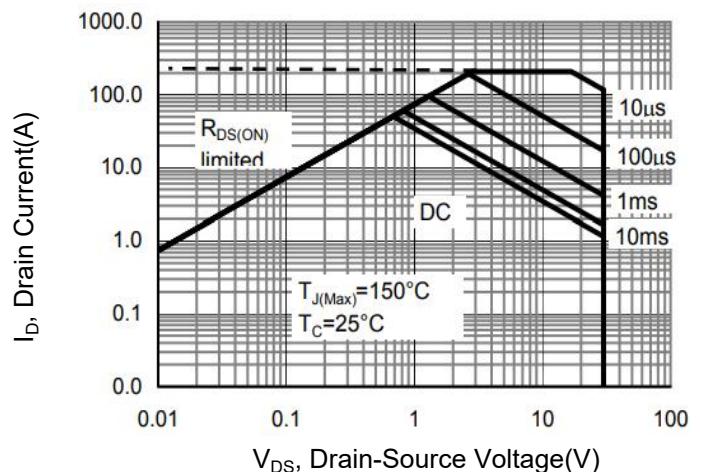
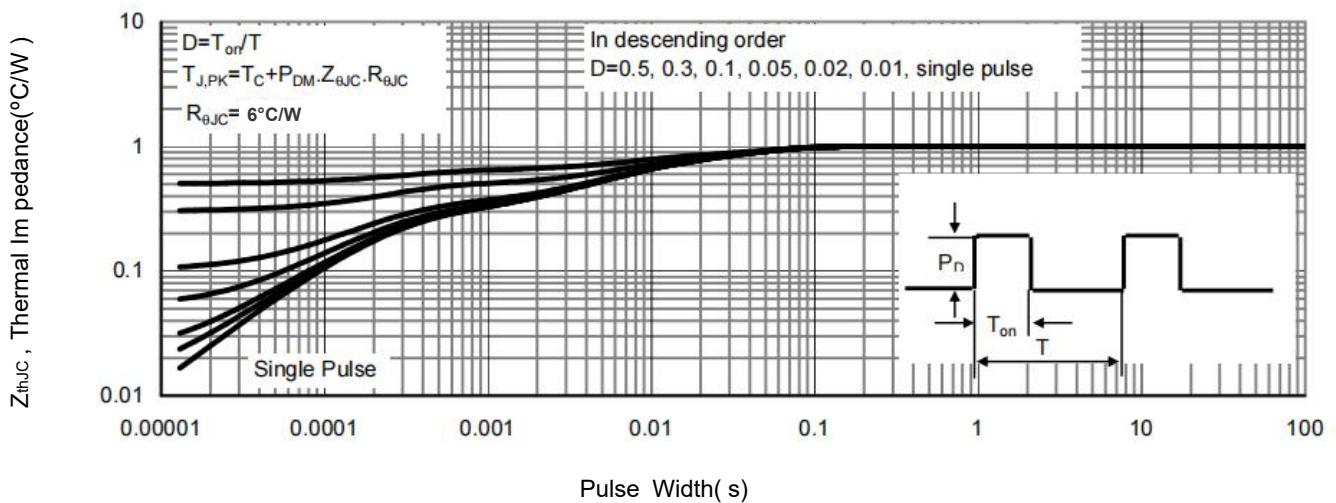
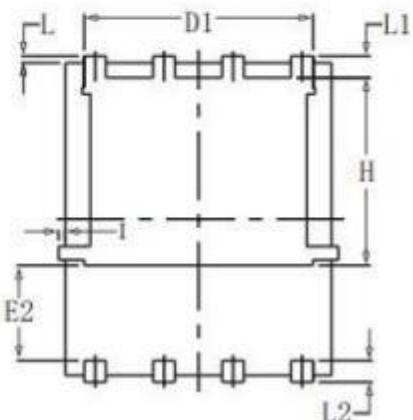
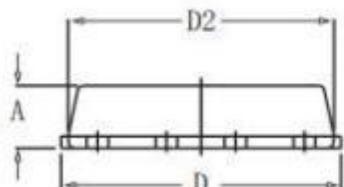
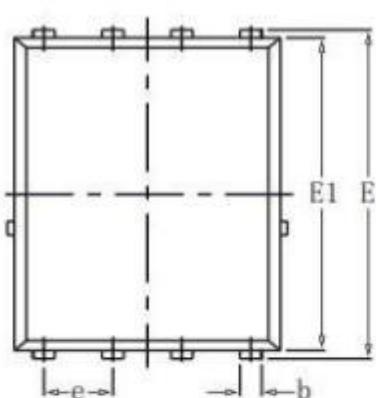


Figure 9 . Normalized MaximumTransient Thermal Impedance



DFN5×6-8L Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	-	0.0630	-
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	-	0.18	-	0.0070