

Features

- Temperature ranges
 - Industrial: -40 °C to 85 °C
- Pin and function compatible with CY7C1041BV33
- High speed
 - $t_{AA} = 8$ ns
- Low active power
 - 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 44-pin TSOP II package

Functional Description

The CY7C1041CV33 is a high performance CMOS static RAM organized as 262,144 words by 16 bits.

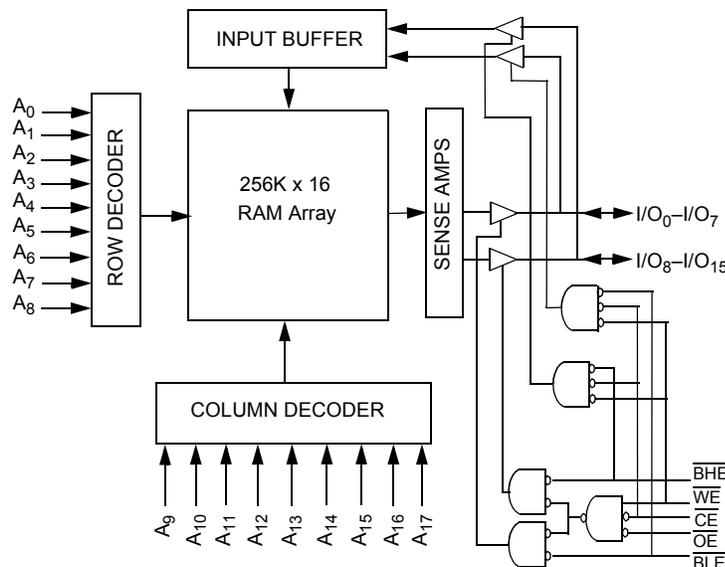
To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from IO pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . For more information, see the [Truth Table on page 10](#) for a complete description of Read and Write modes.

The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

For a complete list of related documentation, click [here](#).

Logic Block Diagram



Contents

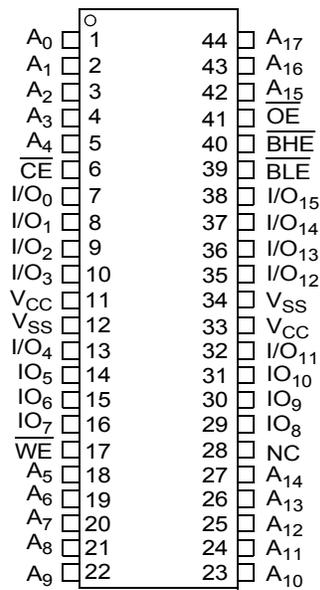
Selection Guide	3	Ordering Code Definitions	12
Pin Configurations	3	Package Diagram	13
Pin Definitions	4	Acronyms	14
Maximum Ratings	5	Document Conventions	14
Operating Range	5	Units of Measure	14
Electrical Characteristics	5	Document History Page	15
Capacitance	6	Sales, Solutions, and Legal Information	17
Thermal Resistance	6	Worldwide Sales and Design Support	17
AC Test Loads and Waveforms	6	Products	17
Switching Characteristics	7	PSoC® Solutions	17
Switching Waveforms	8	Cypress Developer Community	17
Truth Table	11	Technical Support	17
Ordering Information	12		

Selection Guide

Description	-8	Unit
Maximum Access Time	8	ns
Maximum Operating Current	100	mA
Maximum CMOS Standby Current	10	mA

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) ^[1]



Note

1. NC pins are not connected on the die.

Pin Definitions

Pin Name	TSOP Pin Number	I/O Type	Description
A ₀ -A ₁₇	1-5, 18-27, 42-44	Input	Address Inputs. Used to select one of the address locations.
I/O ₀ -I/O ₁₅	7-10, 13-16, 29-32, 35-38	Input or Output	Bidirectional Data IO lines. Used as input or output lines depending on operation.
NC	28	No Connect	No Connects. Not connected to the die.
$\overline{\text{WE}}$	17	Input or Control	Write Enable Input, Active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{\text{CE}}$	6	Input or Control	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	Input or Control	Byte Write Select Inputs, Active LOW. $\overline{\text{BHE}}$ controls I/O ₁₅ -I/O ₈ , $\overline{\text{BLE}}$ controls I/O ₇ -I/O ₀ .
$\overline{\text{OE}}$	41	Input or Control	Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tri-stated and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the Device. Connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply Inputs to the Device.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage on V _{CC} Relative to GND ^[2]	-0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5 V to V _{CC} + 0.5 V

DC Input Voltage ^[2]	-0.5 V to V _{CC} + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch Up Current	> 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Industrial	-40 °C to +85 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-8		Unit
			Min	Max	
V _{OH}	Output HIGH Voltage	V _{CC} = Min, I _{OH} = -4.0 mA	2.4	-	V
V _{OL}	Output LOW Voltage	V _{CC} = Min, I _{OL} = 8.0 mA	-	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL} ^[2]	Input LOW Voltage		-0.3	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output disabled	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, f = f _{MAX} = 1/t _{RC}	-	100	mA
I _{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	-	40	mA
I _{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	-	10	mA

Note

2. V_{IL} (min) = -2.0 V and V_{IH} (max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.

Capacitance

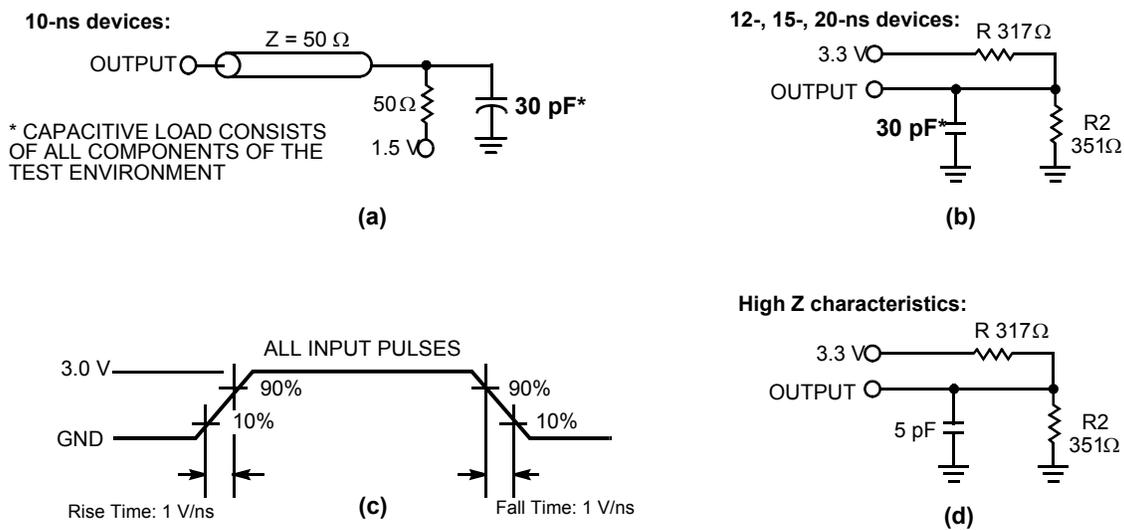
Parameter ^[3]	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	TSOP II	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	42.96	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		10.75	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 2 (a). All other speeds are tested using the Thevenin load shown in Figure 2 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (d).

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description	-8		Unit
		Min	Max	
Read Cycle				
$t_{power}^{[6]}$	V_{CC} (Typical) to the First Access	100	–	μ s
t_{RC}	Read Cycle Time	8	–	ns
t_{AA}	Address to Data Valid	–	8	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	\overline{CE} LOW to Data Valid	–	8	ns
t_{DOE}	\overline{OE} LOW to Data Valid	–	5	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[7]	0	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]	–	4	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[7]	3	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]	–	4	ns
t_{PU}	\overline{CE} LOW to Power Up	0	–	ns
t_{PD}	\overline{CE} HIGH to Power Down	–	8	ns
t_{DBE}	Byte Enable to Data Valid	–	5	ns
t_{LZBE}	Byte Enable to Low Z	0	–	ns
t_{HZBE}	Byte Disable to High Z	–	5	ns
Write Cycle ^[9, 10]				
t_{WC}	Write Cycle Time	8	–	ns
t_{SCE}	\overline{CE} LOW to Write End	6	–	ns
t_{AW}	Address Setup to Write End	6	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	\overline{WE} Pulse Width	6	–	ns
t_{SD}	Data Setup to Write End	4	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]	–	4	ns
t_{BW}	Byte Enable to End of Write	6	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
- t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 2 on page 6. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW, and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} , and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum Write cycle time for Write Cycle No. 3 (WE Controlled, OE LOW) is the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

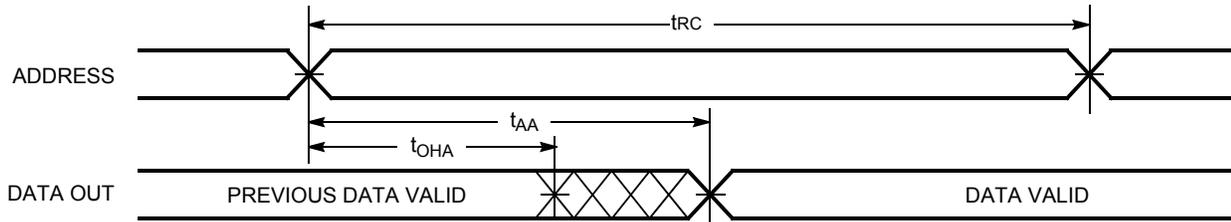
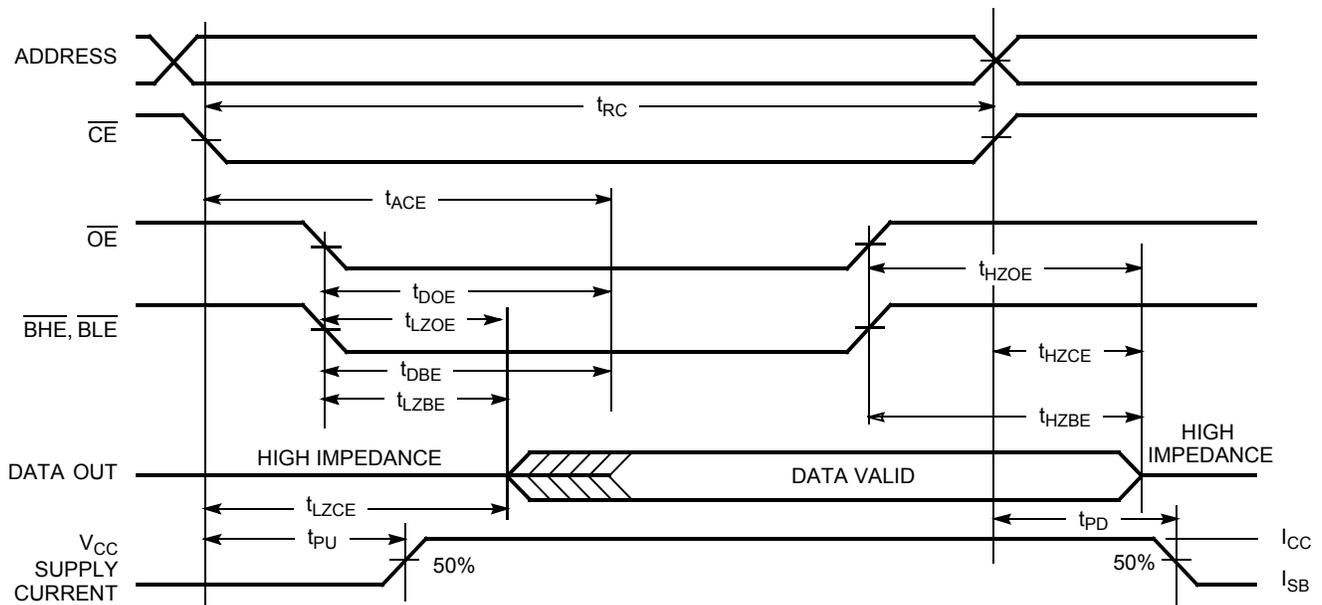


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]



Notes

- 11. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and/or $\overline{BLE} = V_{IL}$.
- 12. \overline{WE} is HIGH for read cycle.
- 13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [14, 15]

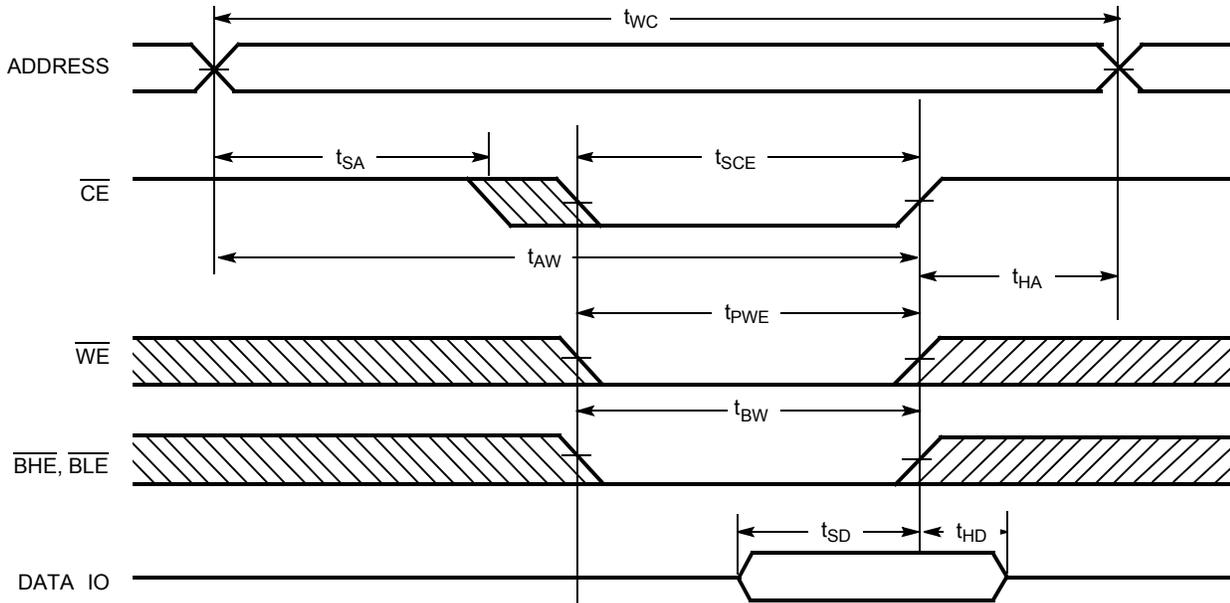
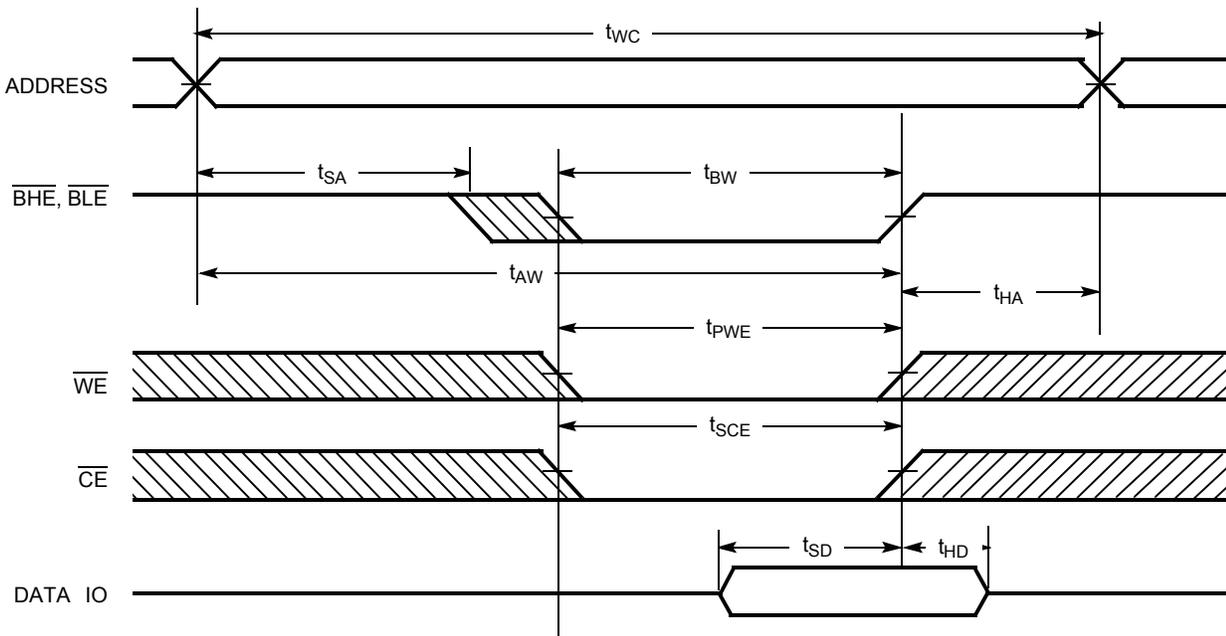


Figure 6. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

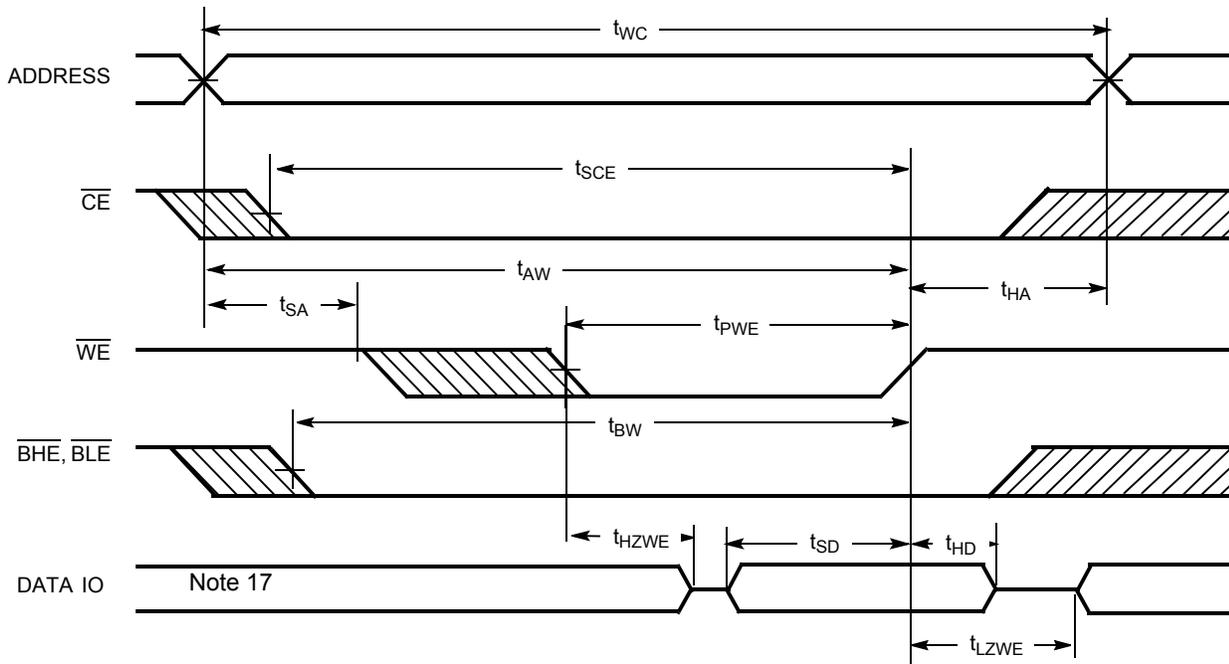


Notes

14. Data IO is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) ^[16]

Notes

16. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE} .
 17. During this time I/Os are in output state. Do not apply input signal.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I _{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I _{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I _{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I _{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

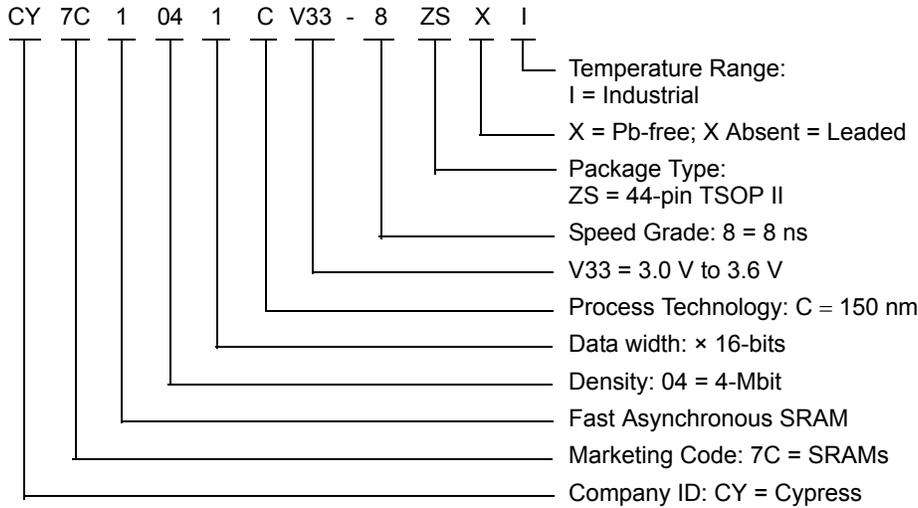
Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer’s representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1041CV33-8ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial

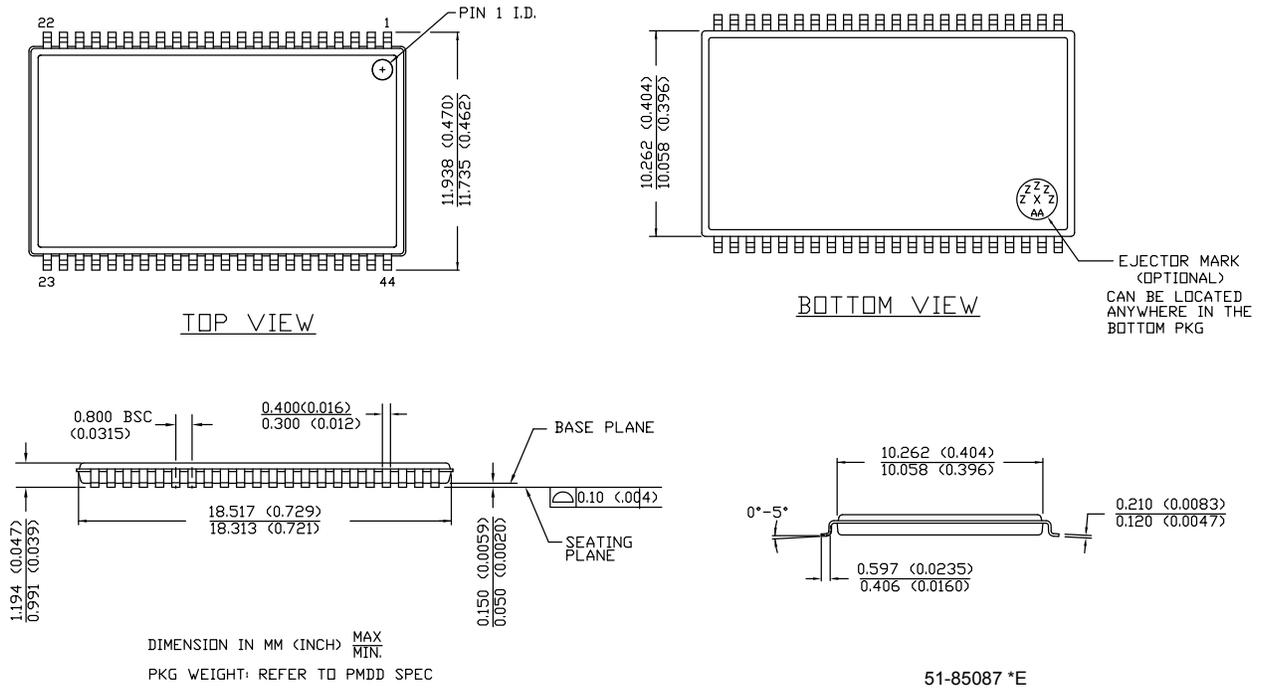
Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions



Package Diagram

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
\overline{OE}	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1041CV33, 4-Mbit (256 K × 16) Static RAM Document Number: 38-05134				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	109513	12/13/01	HGK	New data sheet
*A	112440	12/20/01	BSS	Updated 51-85106 from revision *A to *C
*B	112859	03/25/02	DFP	Added CY7C1042CV33 in BGA package Removed 1042 BGA option pin ACC Final Data Sheet
*C	116477	09/16/02	CEA	Add applications foot note to data sheet
*D	119797	10/21/02	DFP	Added 20-ns speed bin
*E	262949	See ECN	RKF	1) Added Lead (Pb)-Free parts in the Ordering info (Page #9) 2) Added Automotive Specs to Datasheet
*F	361795	See ECN	SYT	Added Pb-Free offerings in the Ordering Information
*G	435387	See ECN	NXR	Removed -8 Speed bin from Product offering. Corrected typo in description for BHE/BLE in pin definitions table on Page# 3 corrected their Pin name from OE2 to OE. Included the Maximum Ratings for Static Discharge Voltage and Latch up Current. Changed the description of I _{I_X} current from Input Load Current to Input Leakage Current Added note# 4 on page# 4 Updated the Ordering Information table
*H	499153	See ECN	NXR	Added Automotive-A Operating Range Changed t _{power} value from 1 μs to 100 μs Updated Ordering Information table
*I	2104110	See ECN	VKN/AESA	Added Automotive-E specs for 12 ns speed Updated Ordering Information table
*J	2897141	03/22/10	AJU/VIVG	Updated Ordering Information (Removed inactive parts). Updated Package Diagram .
*K	3072834	11/12/2010	PRAS	Updated Ordering Information : Removed inactive parts. Added Ordering Code Definitions .
*L	3186840	03/03/2011	PRAS	Updated Features . Updated Selection Guide (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices). Removed Figure “48-Ball FBGA Pinout (Top View)” and renamed Figure “44-Pin SOJ/TSOP II (Top View)” as “44-pin TSOP II (Top View)” in Pin Configurations . Updated Pin Definitions (Deleted the column “BGA Pin Number” and renamed the column “SOJ, TSOP Pin Number” as “TSOP Pin Number”). Updated Operating Range Updated Electrical Characteristics (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices). Updated Thermal Resistance (Deleted the columns SOJ and FBGA). Updated Switching Characteristics (Added -8 ns speed grade devices and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices). Updated Ordering Information (Added new speed bin (-8 ns speed grade devices) and removed -10 ns, -12 ns, -15 ns and -20 ns speed grade devices). Added Acronyms and Units of Measure . Dislodged Automotive information to new datasheet (001-67307) Removed SOJ and FBGA package related information in all instances in the document. Updated to new template.

Document History Page *(continued)*

Document Title: CY7C1041CV33, 4-Mbit (256 K × 16) Static RAM				
Document Number: 38-05134				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*M	3199948	03/18/2011	PRAS	Updated Features (Updated Operating Temperature Range from Commercial to Industrial). Updated Operating Range (Updated Operating Temperature Range from Commercial to Industrial). Updated Ordering Information (Updated Operating Temperature Range from Commercial to Industrial).
*N	3266084	05/28/2011	PRAS	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.").
*O	4315741	03/20/2014	VINI	Updated Package Diagram : spec 51-85087 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*P	4578447	01/16/2015	VINI	Added related documentation hyperlink in page 1. Updated Switching Waveforms : Added Note 16 and referred the same note in Figure 7 .
*Q	4702949	03/27/2015	VINI	Updated Switching Waveforms : Added Note 17 and referred the same note in DATA IO in Figure 7 . Completing Sunset Review.
*R	5962455	11/09/2017	AESATMP8	Updated logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM [®] Cortex [®] Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmhc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2001-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.