Keywords: APD, bias, DS1841, temperature compensation, boost, step-up

APPLICATION NOTE 4221

How to Optimize Avalanche Photodiode (APD) Bias Range Using a DS1841 Logarithmic Resistor

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Abstract: This article describes how three external resistors on the DS1841 logarithmic resistor are used to adjust the output range of an APD bias circuit. A spreadsheet is supplied that makes the adjustment process easy.

APD Bias Circuit

The DS1841 temperature-controlled, NV, I²C, logarithmic resistor contains one 7-bit logarithmic variable resistor. Used in conjunction with a step-up DC-DC converter, the DS1841 adjusts the bias voltage applied to an avalanche photodiode (APD). Three external resistors (R_{SER}, R_{TOP}, and R_{PAR}) are used to adjust the output range (**Figure 1**).

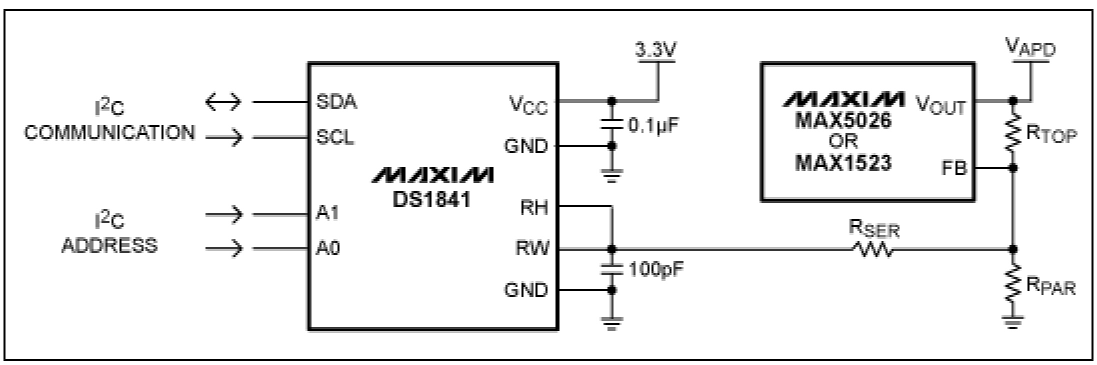

Figure 1. APD bias circuit using the DS1841 and a step-up DC-DC, here the MAX5026 or MAX1523.

Adjusting the APD Bias Range

A spreadsheet, DS1841 APD Bias Range Adjustment (xls), makes it easy to adjust the APD bias range. The spreadsheet has four input variables: R_{TOP}, R_{SER}, R_{PAR}, and V_{FB}. After inputting these resistor values, the spreadsheet then calculates four outputs: V_{APD} (max), V_{APD} (min), STEP (max), STEP (avg). It also generates two graphs: APD Bias vs. DAC Code, Volts Per Step vs. DAC Code. The interface in Figure 2 shows the four variables and the graphics generated from the values input there. **Table 1** defines the terms used in the spreadsheet.

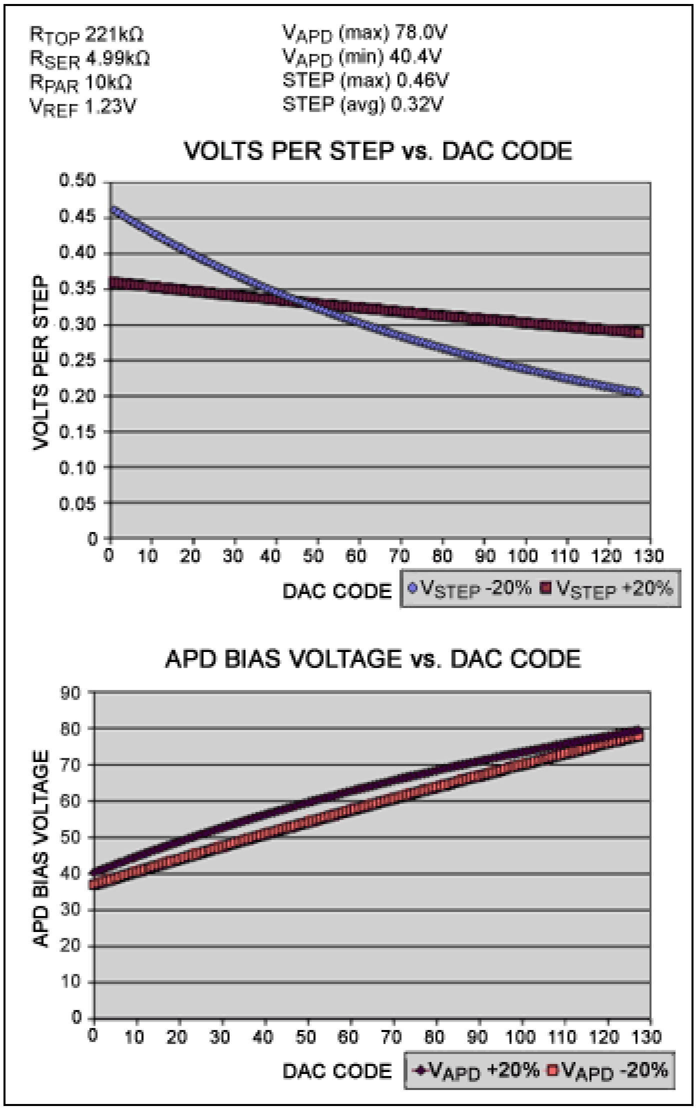

Figure 2. The spreadsheet interface with the four variables for data input, which appear at the top left.

Table 1. Variable Definitions for APD Bias Range Adjustment with the DS1841

V_{FB}	The voltage present at the feedback node of the DC-DC converter.
V_{APD} (max)	The maximum voltage to which the APD bias can be set under worst-case conditions.
V_{APD} (min)	The minimum voltage to which the APD bias can be set under worst-case conditions.
STEP (max)	The maximum calculated voltage step that can occur between two adjacent DAC codes.
STEP (avg)	The average voltage step size that occurs across the full range.
V_{STEP} +20%	The voltage step size when the variable resistor is at the maximum of the process range (+20%).
V_{STEP} -20%	The voltage step size when the variable resistor is at the minimum of the process range (-20%).
V_{APD} +20%	The APD bias voltage when the variable resistor is at the maximum of the process range (+20%).

V_{APD} -20%	The APD bias voltage when the variable resistor is at the minimum of the process range (-20%).

Related Parts		
DS1841	Temperature-Controlled, NV, I²C, Logarithmic Resistor	Free Samples
MAX1523	Simple SOT23 Boost Controllers	Free Samples
MAX5026	500kHz, 36V Output, SOT23, PWM Step-Up DC-DC Converters	Free Samples

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