

MOSFET – Power, Single P-Channel

-40 V, -30 A, 20.5 mΩ

FDWS9511L-F085

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-40	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	-30	A
		$T_C = 100^\circ\text{C}$		-30	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^\circ\text{C}$	P_D	68.2	W
		$T_C = 100^\circ\text{C}$		34.1	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	-9.1	A
		$T_C = 100^\circ\text{C}$		-6.5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_C = 25^\circ\text{C}$	P_D	3.0	W
		$T_C = 100^\circ\text{C}$		1.5	
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	-298	A	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	-100	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = -25$)		E_{AS}	25	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

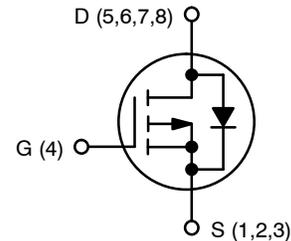
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	2.2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	50	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by wirebond configuration
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-40 V	20.5 mΩ @ -10 V	-30 A
	32.0 mΩ @ -4.5 V	



P-Channel MOSFET



MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- WL = Assembly Lot
- FDWS = Device Code
- 9511L = Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
FDWS9511L-F085	DFNW8 (Power56) (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -40 V	T _J = 25°C		-1	μA
			T _J = 175°C		-1	mA
Zero Gate Voltage Drain Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±16 V			±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1	-1.8	-3	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-5.1		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -30 A	17	20.5	mΩ
		V _{GS} = -4.5 V	I _D = -15 A	26	34	

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 100 KHz, V _{DS} = -20 V		1200		pF
Output Capacitance	C _{OSS}			470		
Reverse Transfer Capacitance	C _{RSS}			26		
Gate Resistance	R _G	V _{GS} = 0.5 V, f = 1 MHz		37		Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -20 V; I _D = -30 A		8		nC
		V _{GS} = -10 V, V _{DS} = -20 V; I _D = -30 A		18		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 0 to -1 V		1		
Gate-to-Source Gate Charge	Q _{GS}	V _{DD} = -20 V, I _D = -30 A		4		
Gate-to-Drain "Miller" Charge	Q _{GD}			3		
Plateau Voltage	V _{GP}			-3.8		V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(ON)}	V _{DD} = -20 V, I _D = -30 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		8		ns
Turn-On Rise Time	t _r			28		
Turn-Off Delay Time	t _{d(OFF)}			112		
Turn-Off Fall Time	t _f			40		

DRAIN-SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Voltage	V _{SD}	I _{SD} = -30 A, V _{GS} = 0 V		-0.9	-1.3	V
		I _{SD} = -15 A, V _{GS} = 0 V		-0.85	-1.2	
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, I _S = -30 A		36		ns
Charge Time	t _a			18		
Discharge Time	t _b			18		
Reverse Recovery Charge	Q _{RR}			24		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

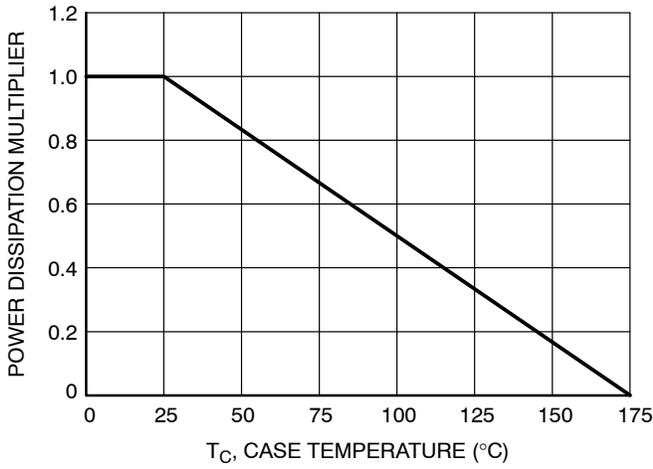


Figure 1. Normalized Power Dissipation vs. Case Temperature

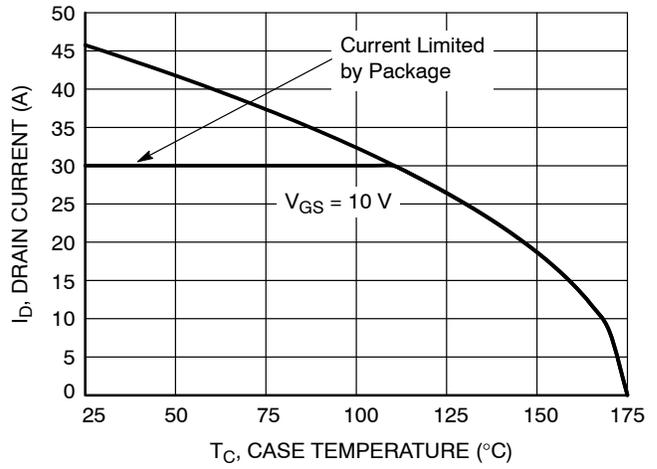


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

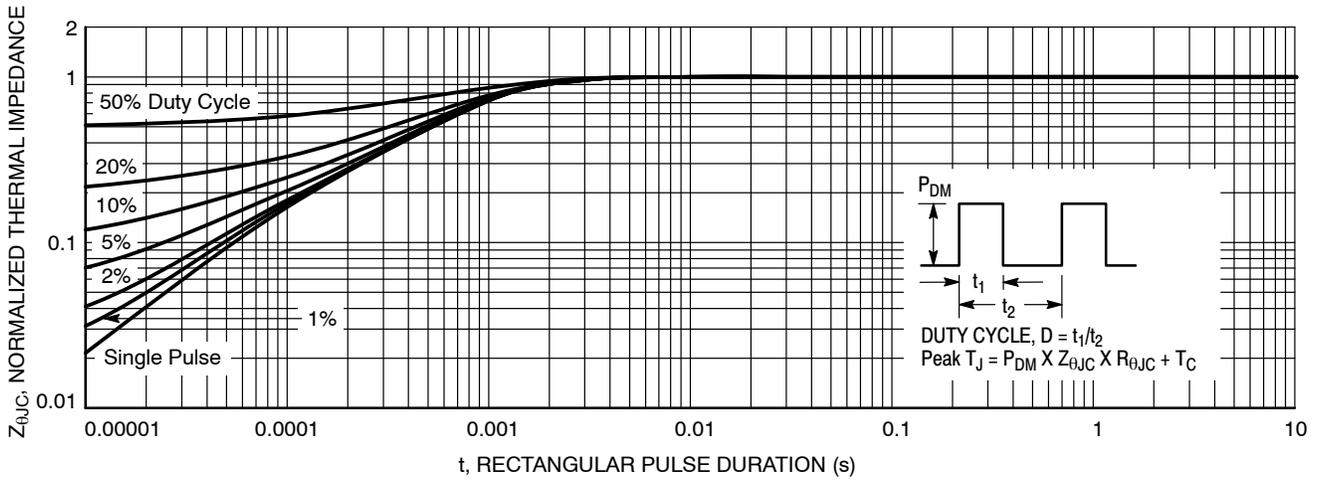


Figure 3. Normalized Maximum Transient Thermal Impedance

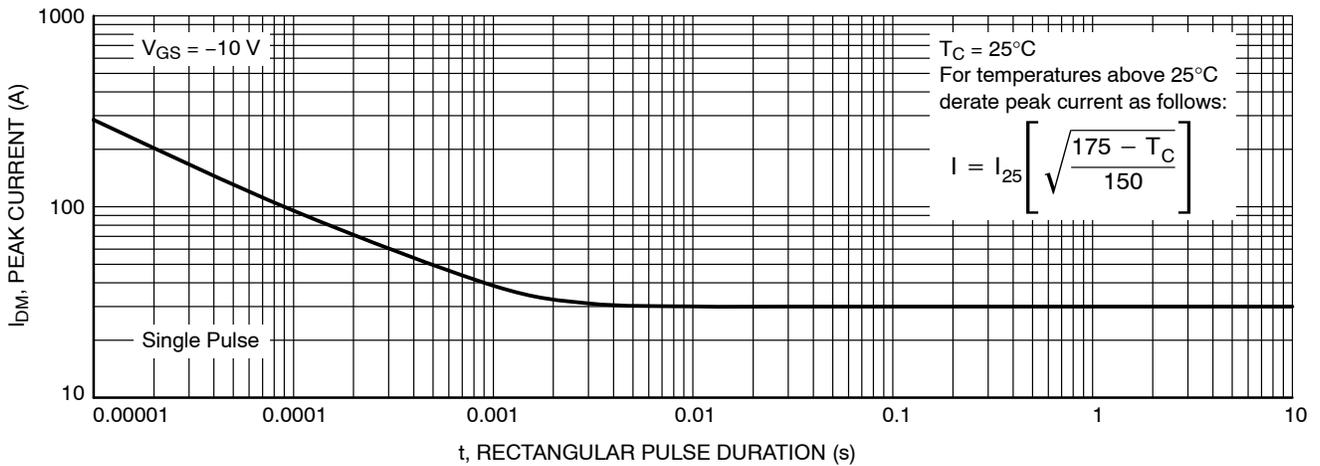


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

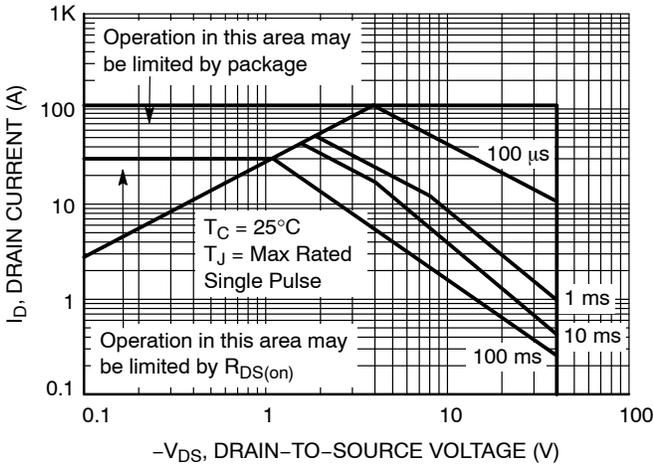


Figure 5. Forward Bias Safe Operating Area

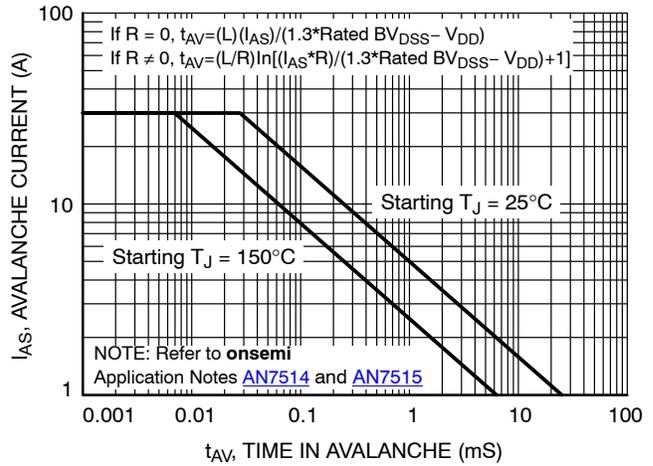


Figure 6. Unclamped Inductive Switching Capability

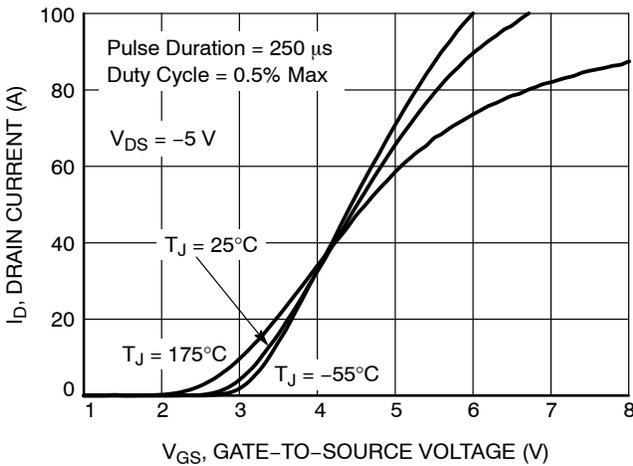


Figure 7. Transfer Characteristics

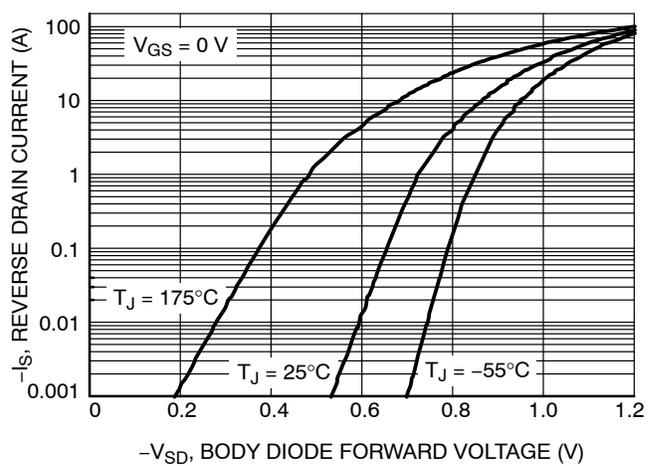


Figure 8. Forward Diode Characteristics

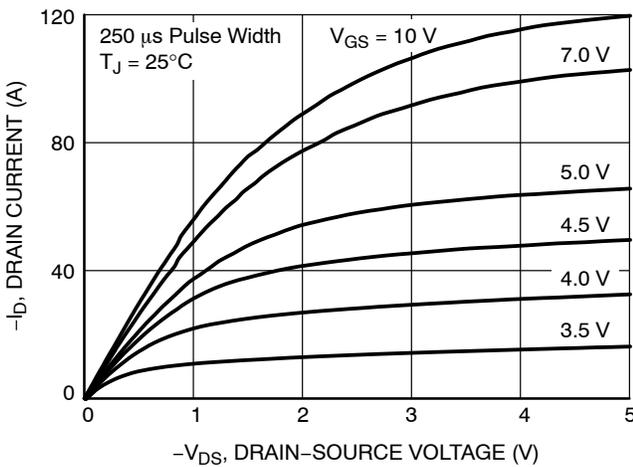


Figure 9. Saturation Characteristics

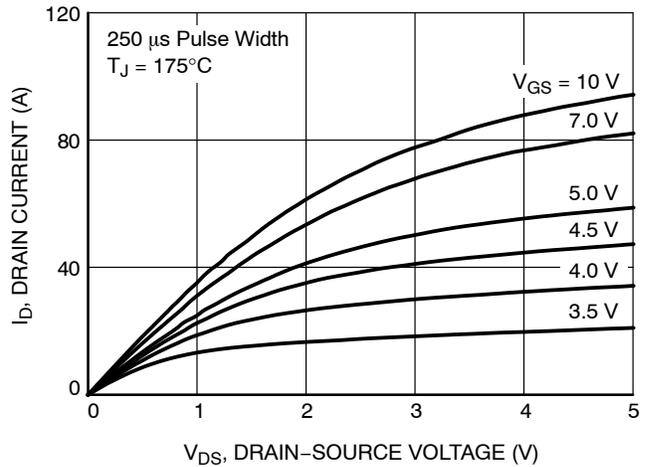


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

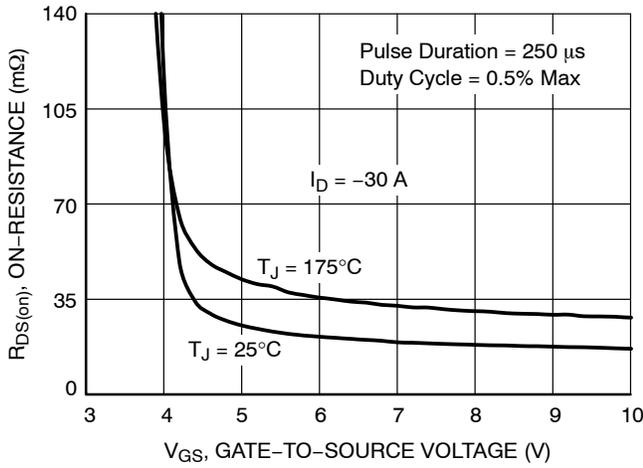


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

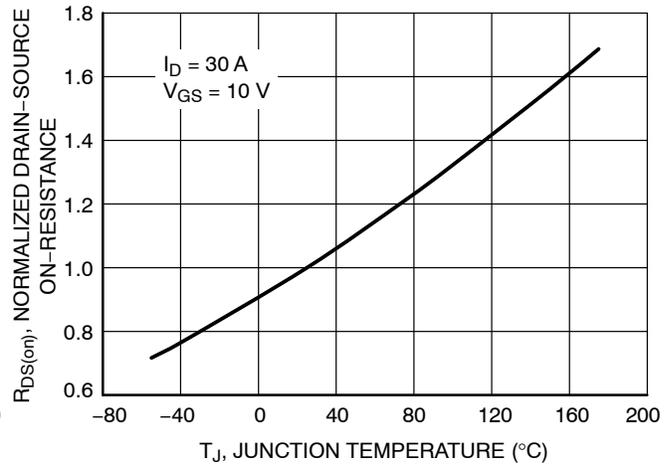


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

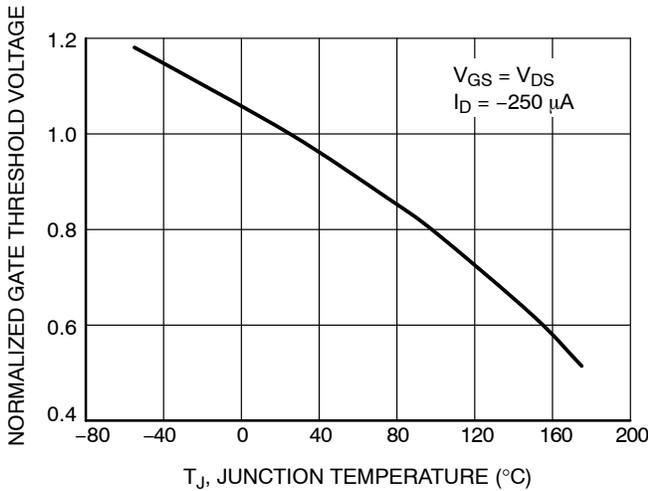


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

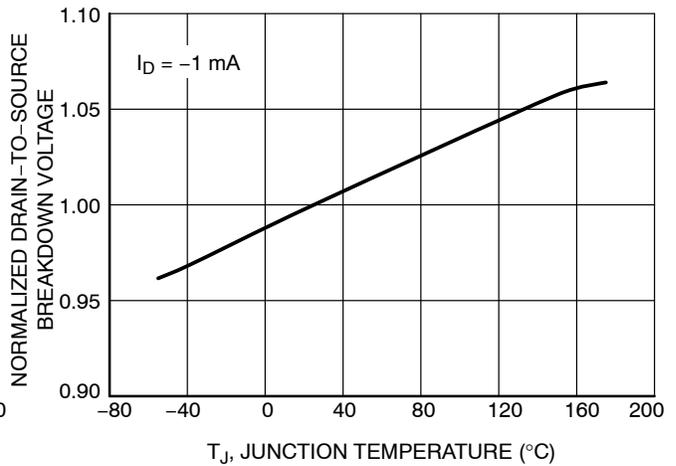


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

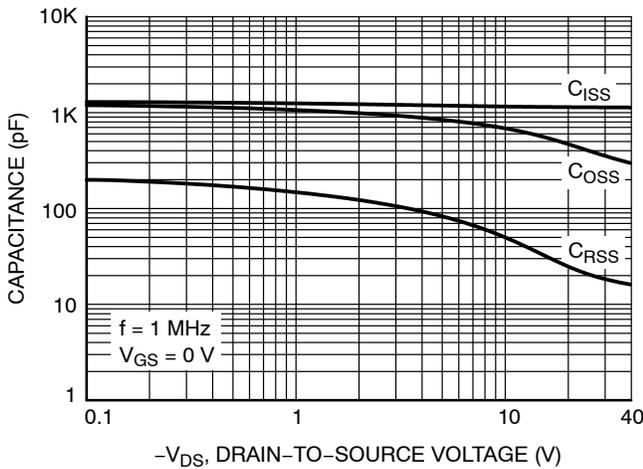


Figure 15. Capacitance vs. Drain-to-Source Voltage

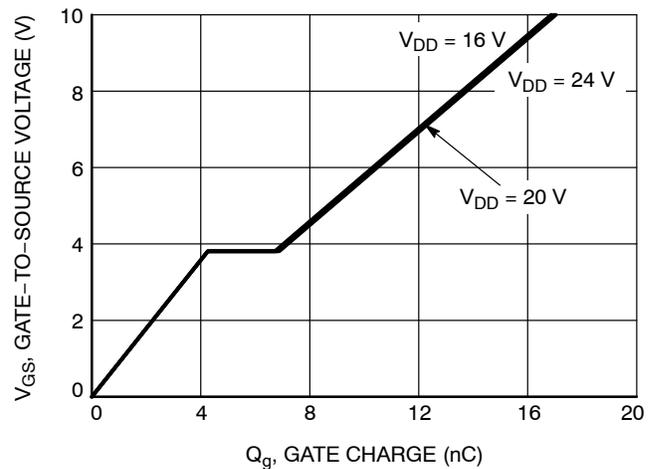
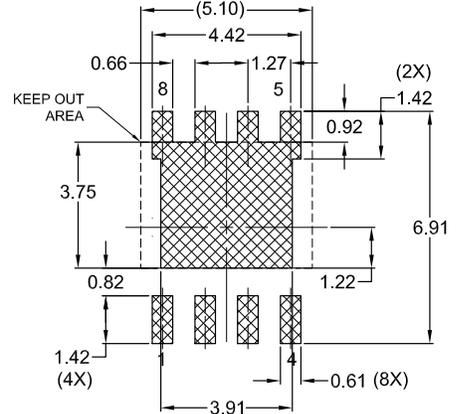
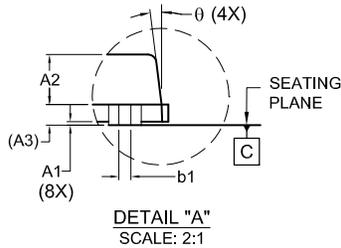
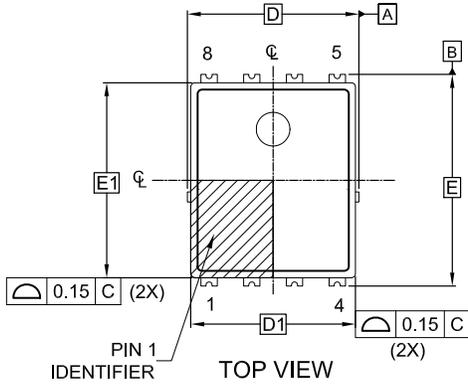


Figure 16. Gate Charge vs. Gate-to-Source Voltage

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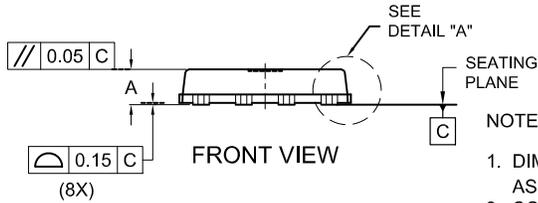
PACKAGE DIMENSIONS

DFNW8 5.2x6.3, 1.27P
CASE 507AU
ISSUE A



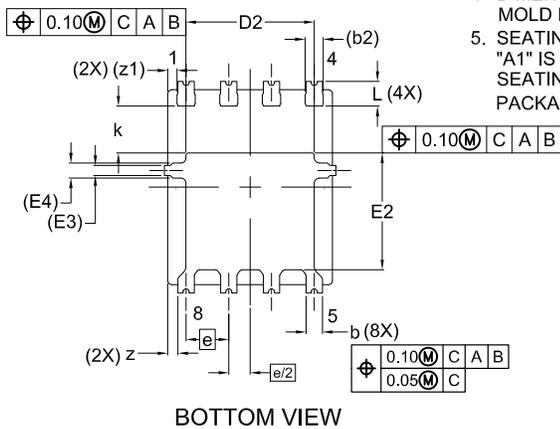
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	-	-	0.05
A2	0.65	0.75	0.85
A3	0.30 REF		
b	0.47	0.52	0.57
b1	0.13	0.18	0.23
b2	(0.54)		
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30 REF		
E4	0.45 REF		
e	1.27 BSC		
e/2	0.635BSC		
k	1.30	1.40	1.50
L	0.64	0.74	0.84
z	0.24	0.29	0.34
z1	(0.28)		
θ	0°	---	12°

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