DATA SHEET
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MOSFET - N-Channel, POWERTRENCH®, DUAL COOL® 56 Shielded Gate

100 V, 60 A, 7.5 mΩ

FDMS86101DC

General Description

This N−Channel MOSFET is produced using **onsemi's** advanced POWERTRENCH® process that incorporates Shielded Gate technology. Advancements in both silicon and DUAL COOL® package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction−to−Ambient thermal resistance.

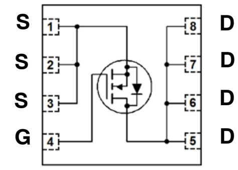
Features

- Shielded Gate MOSFET Technology
- DUAL COOL Top Side Cooling PQFN package
- Max $R_{DS(on)}$ = 7.5 mΩ at V_{GS} = 10 V, I_D = 14.5 A
- Max $R_{DS(on)}$ = 12 mΩ at V_{GS} = 6 V, I_D = 11.5 A
- High performance technology for extremely low $R_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

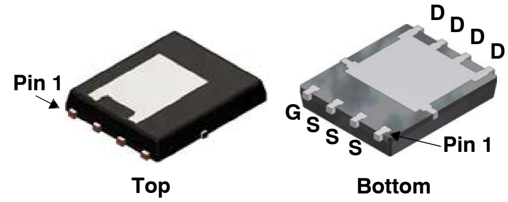
Typical Applications

- Primary DC−DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch

ELECTRICAL CONNECTION

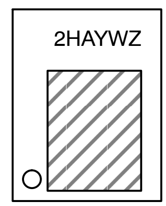


N-Channel MOSFET



DFN8 5.1x6.15
(Dual Cool 56)
CASE 506EG

MARKING DIAGRAM



2H	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
Z	= Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
86101	FDMS86101DC	UDFN8	13”	12 mm	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter				Ratings	Units
V_{DS}	Drain to Source Voltage				100	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	−Continuous	T_C = 25°C		60	A
		−Continuous	T_A = 25°C	(Note 1a)	14.5	
		−Pulsed			200	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	216	mJ
P_D	Power Dissipation		T_C = 25°C		125	W
	Power Dissipation		T_A = 25°C	(Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 14.5 A		6	7.5	mΩ
		V_{GS} = 6 V, I_D = 11.5 A		8.3	12	
		V_{GS} = 10 V, I_D = 14.5 A, T_J = 125°C		10	13	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 14.5 A		44		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		2354	3135	pF
C_{OSS}	Output Capacitance			467	625	pF
C_{RSS}	Reverse Transfer Capacitance			23	35	pF
R_G	Gate Resistance		0.1	1.4	3	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn – On Delay Time	V_{DD} = 50 V, I_D = 14.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		14	25	ns
t_r	Rise Time			8.2	17	ns
$t_{D(OFF)}$	Turn – Off Delay Time			25	40	ns
t_f	Fall Time			5.5	11	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 14.5 A		31	44	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V		18	25	nC
Q_{gs}	Gate to Source Gate Charge			8.3		nC
Q_{gd}	Gate to Drain ”Miller” Charge			7		nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.7 A (Note 2)		0.71	1.2	V
		V_{GS} = 0 V, I_S = 14.5 A (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	I_F = 14.5 A, di/dt = 100 A/μs		54	87	ns
Q_{rr}	Reverse Recovery Charge			62	99	nC

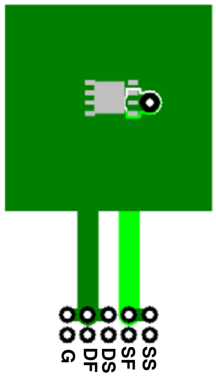
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	13	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR−4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b) 81°C/W when mounted on a minimum pad of 2 oz copper.

c) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

e) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

f) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

g) .200FPM Airflow, No Heat Sink, 1 in^2 pad of 2 oz copper

h) .200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

k) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

l) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 0.3 mH, I_{AS} = 38 A, V_{DD} = 90 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

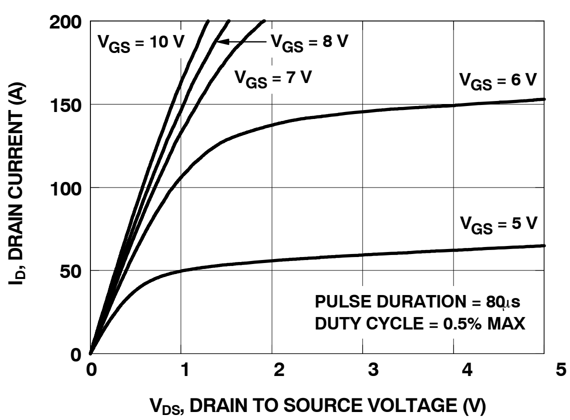


Figure 1. On Region Characteristics

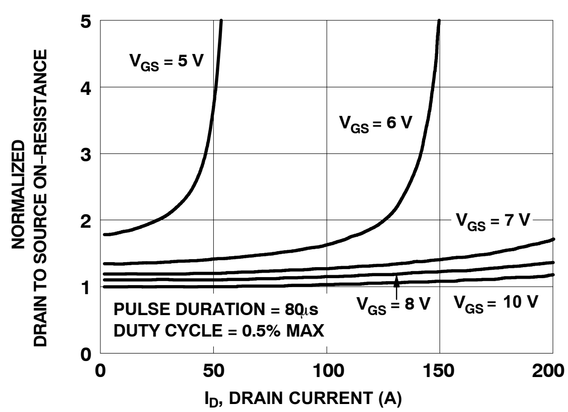


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

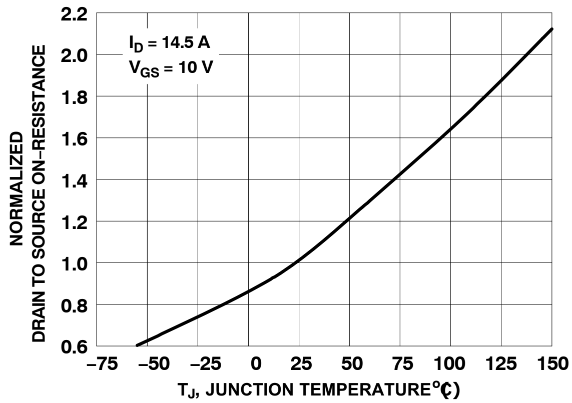


Figure 3. Normalized On Resistance vs. Junction Temperature

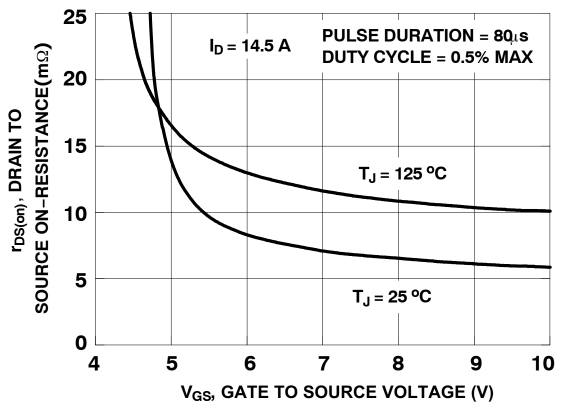


Figure 4. On-Resistance vs. Gate to Source Voltage

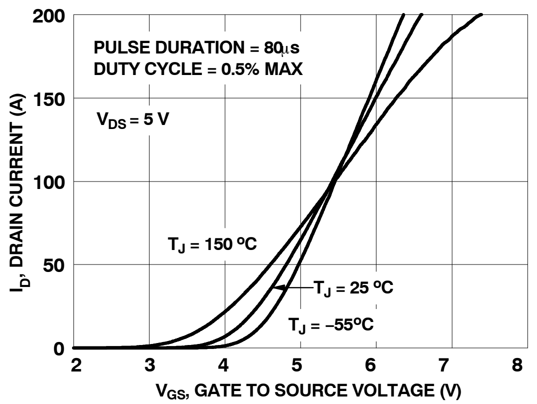


Figure 5. Transfer Characteristics

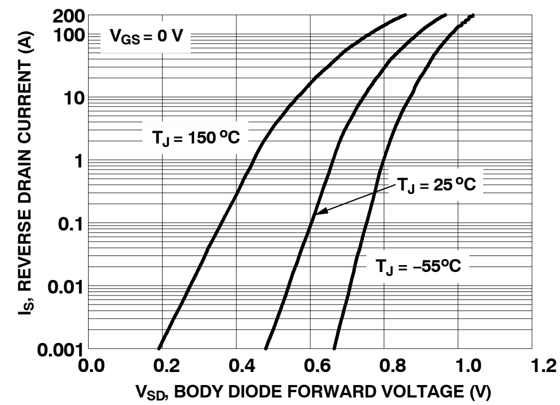


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

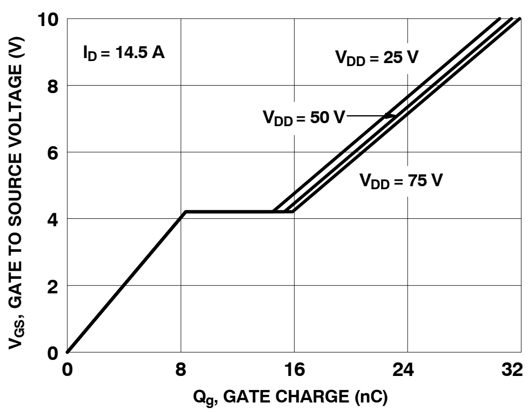


Figure 7. Gate Charge Characteristics

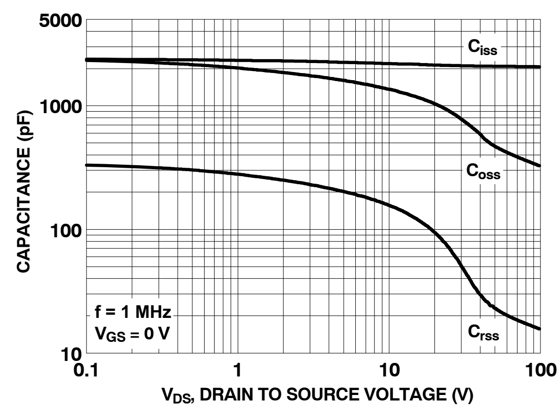


Figure 8. Capacitance vs. Drain to Source Voltage

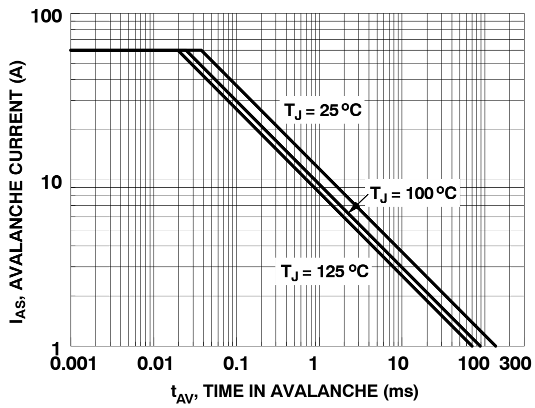


Figure 9. Unclamped Inductive Switching Capability

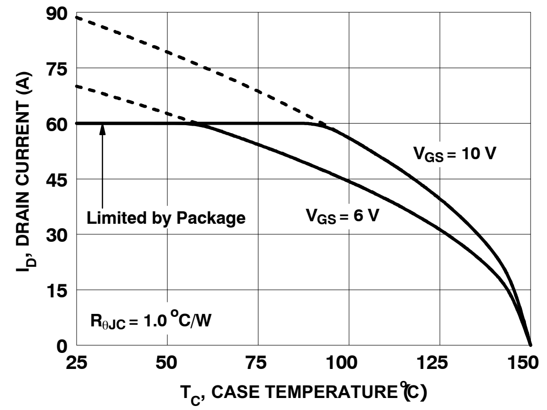


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

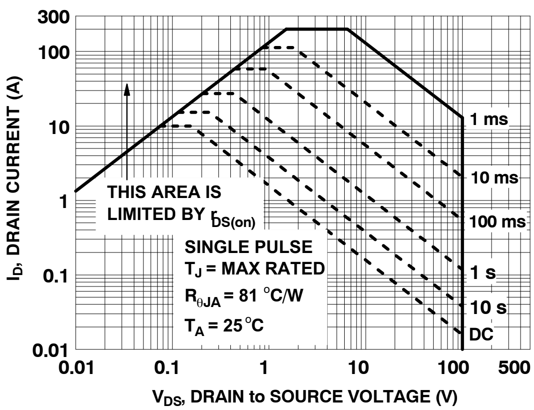


Figure 11. Forward Bias Safe Operating Area

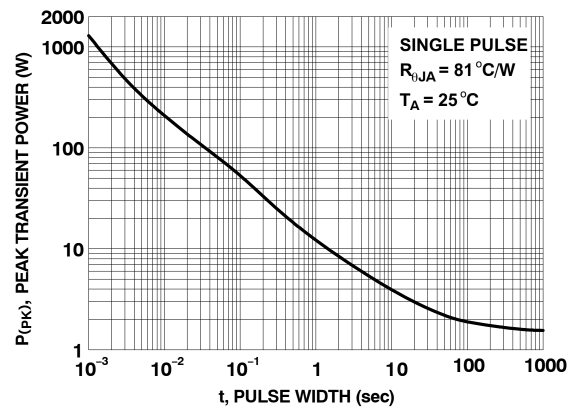


Figure 12. Single Pulse Maximum Power Dissipation

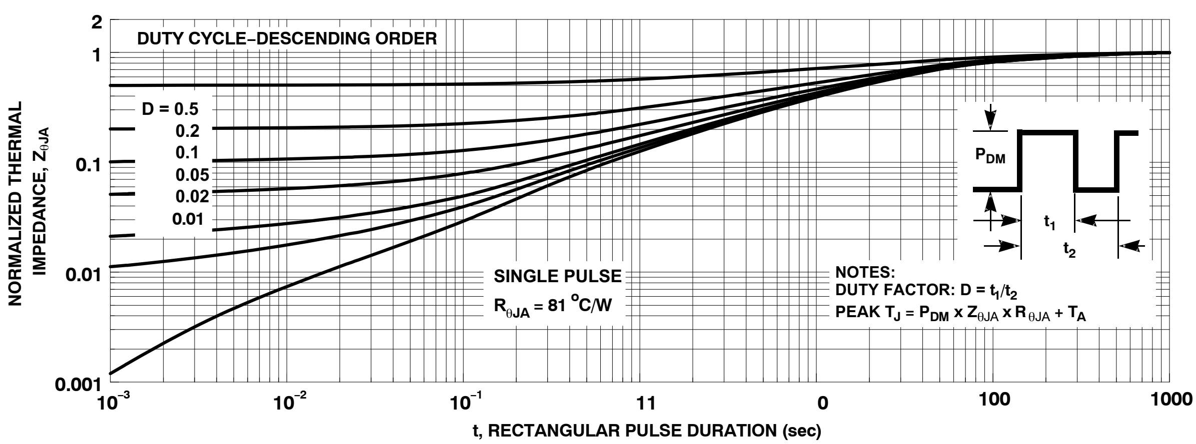


Figure 13. Junction−to−Case Transient Thermal Response Curve

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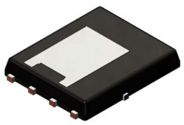
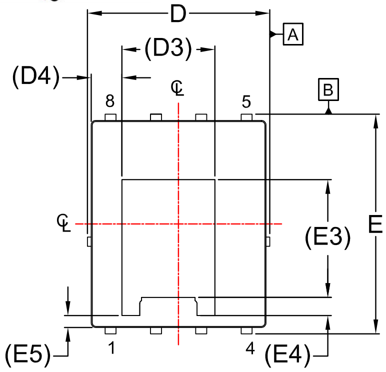
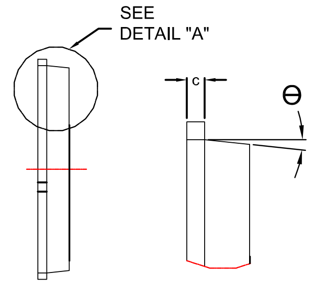
DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

DATE 25 AUG 2020





TOP VIEW

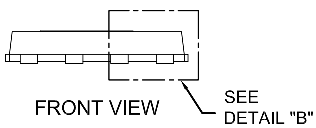


SIDE VIEW

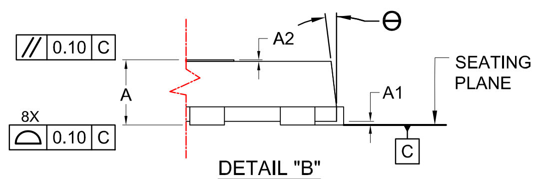
DETAIL "A"
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

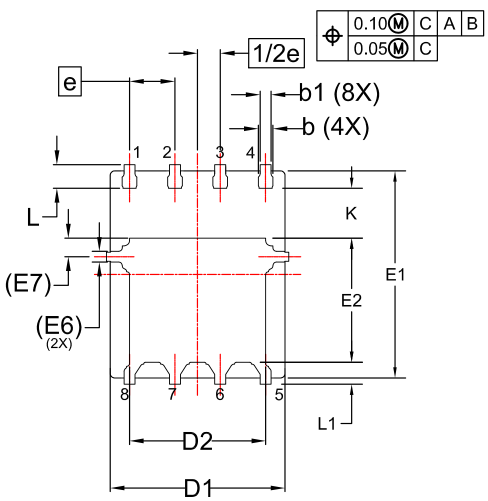


FRONT VIEW

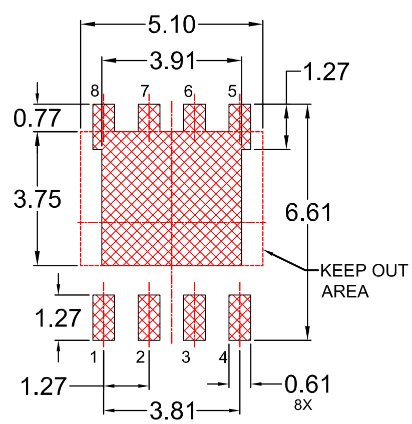


DETAIL "B"
SCALE: 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°



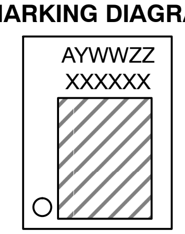
BOTTOM VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON84257G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DFN8 5x6.15, 1.27P, DUAL COOL	PAGE 1 OF 1

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