

Package

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Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET



Top view					
PRODUCT SUMMARY					
V _{DS} (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.00100				
I _D (A)	250				
Configuration	Single				

TO-263-7L

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_q and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



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G _O	
N-Channel MOSFET) S

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V_{GS}	± 20	V	
Continuous drain current	T _C = 25 °C ^a	1	250		
	T _C = 125 °C	ID	229		
Continuous source current (diode conduction) ^a		Is	250	Α	
Pulsed drain current ^b		I _{DM}	420		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	78		
Single pulse avalanche energy	L = 0.1 mm	E _{AS}	304	mJ	
Maximum power dissipation ^b	T _C = 25 °C	D	300	W	
	T _C = 125 °C	P_D	100	VV	
Operating junction and storage temperature	range	T _J , T _{stg}	-55 to +175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-ambient P	PCB mount c	R_{thJA}	40	°C/W	
Junction-to-case (drain)		R_{thJC}	0.5	G/VV	

Notes

- a. Package limited
- b. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty cycle} \leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)



Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static					•	•		
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	2.5	3.0	3.5	V	
Gate-source leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μA	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	500	μΑ	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	100	-	-	Α	
		V _{GS} = 10 V	I _D = 40 A	-	0.00081	0.00100		
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 40 A, T _J = 125 °C	-	-	0.00152	Ω	
		V _{GS} = 10 V	I _D = 40 A, T _J = 175 °C	-	-	0.00184		
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 40 A	-	181	-	S	
Dynamic ^b								
Input capacitance	C _{iss}			-	10 841	15 000		
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	2928	4000	pF	
Reverse transfer capacitance	C _{rss}			-	198	270		
Total gate charge ^c	Qg			-	163	245		
Gate-source charge c	Q_{gs}	$V_{GS} = 10 \text{ V}$ $V_{DS} = 20 \text{ V}, I_D = 100 \text{ A}$		-	46	=	nC	
Gate-drain charge ^c	Q _{gd}]		-	36	-		
Gate resistance	R_g	f = 1 MHz		1	2.2	3.4	Ω	
Turn-on delay time ^c	t _{d(on)}			-	24	40		
Rise time ^c	t _r	V _{DD} =	= 20 V, $R_L = 0.2 \Omega$	-	215	330	no	
Turn-off delay time ^c	t _{d(off)}	$I_D \cong 100 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		-	59	90	ns	
Fall time ^c	t _f			-	35	55		
Source-Drain Diode Ratings and Chara	cteristics ^b							
Pulsed current ^a	I _{SM}			-	-	420	Α	
Forward voltage	V_{SD}	I _F = 60 A, V _{GS} = 0 V		-	0.8	1.5	V	
Body diode reverse recovery time	t _{rr}			-	92	185	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 40 A, di/dt = 100 A/μs		-	198	400	nC	
Reverse recovery fall time	ta			-	47	-	no	
Reverse recovery rise time	t _b			-	45	-	ns	
Body diode peak reverse recovery current	I _{RM(REC)}			_	-4.4	-	Α	

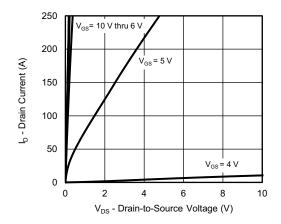
Notes

- a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

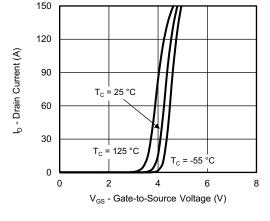
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



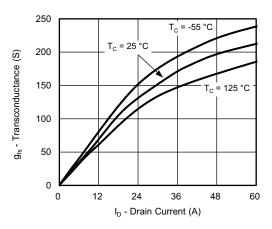
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



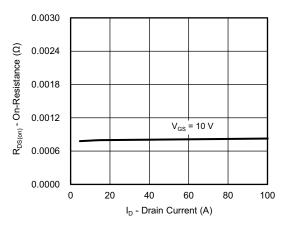
Output Characteristics



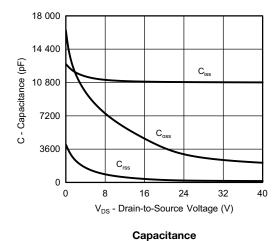
Transfer Characteristics

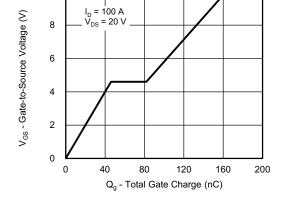


Transconductance



On-Resistance vs. Drain Current

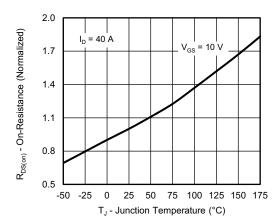




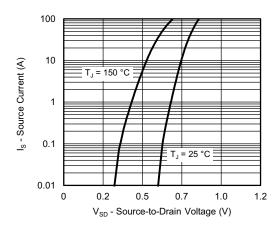
10



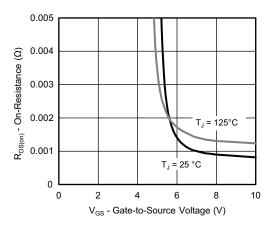
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



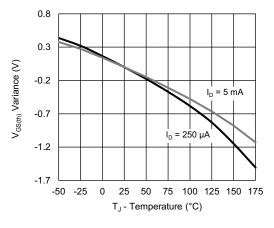
On-Resistance vs. Junction Temperature



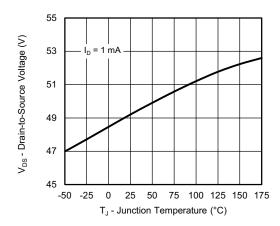
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



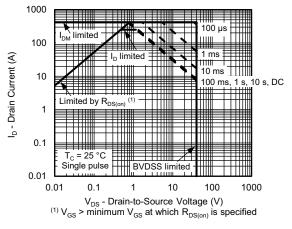
Threshold Voltage



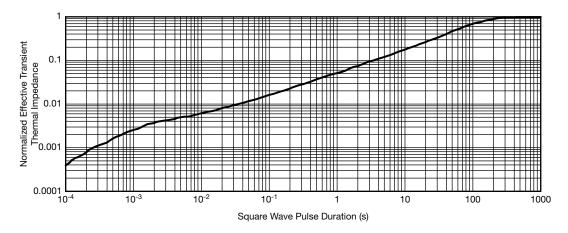
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



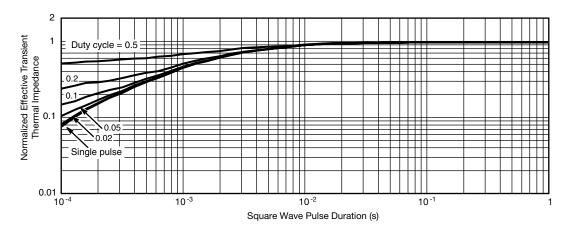
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

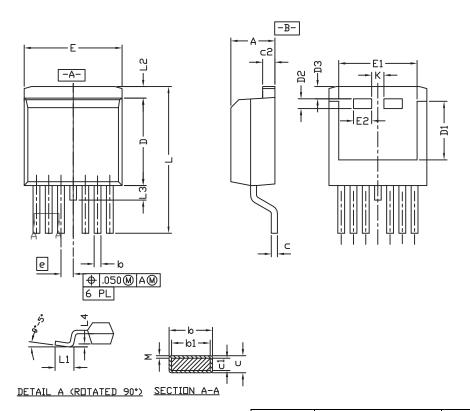
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg276558.





D²PAK (TO-263-7L) Case Outline



Notes

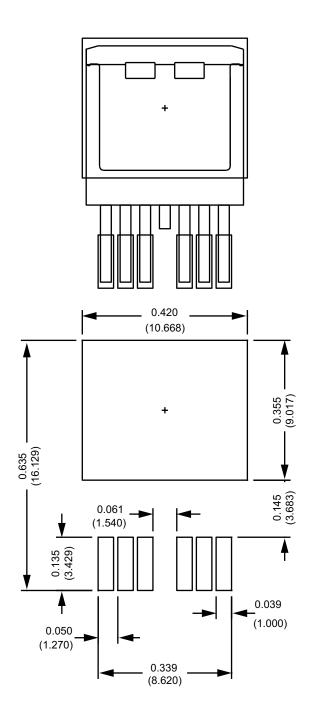
- 1. Plane B includes maximum features of heat sink tab and plastic
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
- 3. Pin to pin coplanarity max. 4 mils
- 4. Lead thickness 25 mils
- 5. For SUM part numbers lead thickness is 24 mils to 29 mils
- 6. For reference only
- 7. Use inches as the primary measurement
- 8. This feature is only for SUM

	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
Α	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.260	0.280	6.604	7.112
D2	0.046	0.050	1.168	1.270
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
е	0.050	BSC	1.27	BSC
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
М	-	0.002	-	0.050
ECN: T22-0410-Rev. D, 19-Sep-2022 DWG: 6006				

Revision: 19-Sep-2022 Document Number: 63782



Recommended Land Pattern D²PAK (TO-263-7L)





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