### **General Description**

The MAX9171/MAX9172 single/dual low-voltage differential signaling (LVDS) receivers are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single 3.3V supply.

The MAX9171 is a single LVDS receiver and the MAX9172 is a dual LVDS receiver. Both devices conform to the ANSI TIA/EIA-644 LVDS standard and convert LVDS to LVTTL/LVCMOS-compatible outputs. A fail-safe feature sets the outputs high when the inputs are undriven and open, terminated, or shorted. The MAX9171/MAX9172 are available in 8-pin SO packages and space-saving thin DFN and SOT23 packages.

For lower skew devices, refer to the MAX9111/ MAX9113 data sheet.

### Applications

Multipoint Backplane Interconnect Laser Printers Digital Copiers Cellular Phone Base Stations LCD Displays Network Switches/Routers Clock Distribution

### \_Features

- Input Accepts LVDS and LVPECL
- In-Path Fail-Safe Circuit
- Space-Saving 8-Pin TDFN and SOT23 Packages
- Fail-Safe Circuitry Sets Output High for Open, Undriven Shorted, or Undriven Terminated Output
- Flow-Through Pinout Simplifies PCB Layout
- Guaranteed 500Mbps Data Rate
- Second Source to DS90LV018A and DS90LV028A (SO Packages Only)
- Conforms to ANSI TIA/EIA-644 Standard
- ♦ 3.3V Supply Voltage
- ♦ -40°C to +85°C Operating Temperature Range
- Low-Power Dissipation

### **Ordering Information**

PART	PIN-PACKAGE	TOP MARK	PKG CODE
MAX9171EKA-T	8 SOT23-8	AALX	K8-1
MAX9171ESA	8 SO	_	S8-2
MAX9171ETA*	8 Thin DFN-EP**	_	T833-2
MAX9172EKA-T	8 SOT23-8	AALY	K8-1
MAX9172ESA	8 SO	_	S8-2
MAX9172ETA*	8 Thin DFN-EP**		T833-2

**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

\*Future product—contact factory for availability.

\*\*EP = Exposed pad.

T = Tape-and-reel.

### Pin Configurations



### 

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

### **ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
ESD Protection	
Human Body Model (IN_+, IN_	)±13kV
Lead Temperature (soldering, 10	)s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 3.0V \text{ to } 3.6V, \text{ differential input voltage } |V_{ID}| = 0.1V \text{ to } 1.2V, \text{ receiver input voltage } = 0 \text{ to } V_{CC}, \text{ common-mode voltage } V_{CM} = |V_{ID}/2| \text{ to } (V_{CC} - |V_{ID}/2|), T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{CC} = 3.3V, |V_{ID}| = 0.2V, V_{CM} = 1.2V, T_A = +25^{\circ}\text{C}.) \text{ (Notes } 1, 2)$ 

PARAMETER	SYMBOL		CONDITIONS	MIN	ТҮР	MAX	UNITS
LVDS INPUTS (IN_+, IN)							
Differential Input High Threshold	V <sub>TH</sub>	Figure 1			-40	0	mV
Differential Input Low Threshold	V <sub>TL</sub>	Figure 1		-100	-40		mV
Input Current (Noninverting Input)	I <sub>IN+</sub>	Figure 1		+0.5	-2.1	-5.0	μΑ
Power-Off Input Current (Noninverting Input)	I <sub>IN+OFF</sub>	$V_{IN+} = 0$ to 3.6 or open (Figure	$V, V_{IN-} = 0 \text{ to } 3.6V, V_{CC} = 0$ e 1)	-0.5	0	+0.5	μA
Input Current (Inverting Input)	I <sub>IN-</sub>	Figure 1		-0.5	+4.4	+10.0	μA
Power-Off Input Current (Inverting Input)	I <sub>IN-OFF</sub>	V <sub>IN+</sub> = 0 to 3.6 or open (Figure	$V, V_{IN-} = 0 \text{ to } 3.6V, V_{CC} = 0$ e 1)	-0.5	0	+0.5	μA
LVCMOS/LVTTL OUTPUTS (OUT	_)	•					
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	Open, undriven short, or undriven parallel termination	2.7	3.2		V
			$V_{ID} = 0V$	2.7	3.2		
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.0mA, V	/ <sub>ID</sub> = -100mV		0.1	0.4	V
Output Short-Circuit Current	IOS	$V_{OUT} = 0$ (No	te 3)	-45	-77	-120	mA
POWER SUPPLY	1	1					1
Supply Current	1		MAX9171		3.6	6	
Supply Current	Icc	Inputs open	MAX9172		7.0	9	mA

### SWITCHING CHARACTERISTICS

(V<sub>CC</sub> = 3.0V to 3.6V, C<sub>L</sub> = 15pF,  $IV_{ID}I$  = 0.2V,  $V_{CM}$  = 1.2V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{CC}$  = 3.3V, T<sub>A</sub> = +25°C.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS
Differential Propagation Delay High to Low	t <sub>PHLD</sub>	Figures 2, 3	1.0	1.65	2.5	ns
Differential Propagation Delay Low to High	<sup>t</sup> PLHD	Figures 2, 3	1.0	1.62	2.5	ns
Differential Pulse Skew ItpHLD - tpLHDI	<sup>t</sup> SKD1	Figures 2, 3 (Note 7)		30	400	ps
Differential Channel-to-Channel Skew (MAX9172)	tskd2	Figures 2, 3 (Note 8)		40	500	ps
Differential Part-to-Part Skew	tskd3	Figures 2, 3 (Note 9)			1	
Differential Part-to-Part Skew	tskD4	Figures 2, 3 (Note 10)			1.5	ns
Rise Time	tтLн	Figures 2, 3		0.55	0.8	ns
Fall Time	tthl	Figures 2, 3		0.51	0.8	ns
Maximum Operating Frequency	fMAX	All channels switching, $V_{OL(MAX)} = 0.4V$ , $V_{OH(MIN)} = 2.7V$ , $40\% < duty cycle < 60\%$	250	300		MHz

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to GND except V<sub>TH</sub>, V<sub>TL</sub>, and V<sub>ID</sub>.

Note 2: All devices are 100% production tested at  $T_A = +25^{\circ}C$  and are guaranteed by design for  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , as specified.

**Note 3:** Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

Note 4: AC parameters are guaranteed by design and not production tested.

Note 5:  $C_L$  includes scope probe and test jig capacitance.

Note 6: Pulse generator output conditions:  $t_R = t_F < 1ns$  (0% to 100%), frequency = 250MHz, 50% duty cycle,  $V_{OH} = 1.3V$ ,  $V_{OL} = 1.1V$ .

**Note 7:** t<sub>SKD1</sub> is the magnitude of the difference of differential propagation delays in a channel. t<sub>SKD1</sub> = lt<sub>PHLD</sub> - t<sub>PLHD</sub>l.

Note 8: t<sub>SKD2</sub> is the magnitude of the difference of the t<sub>PLHD</sub> or t<sub>PHLD</sub> of one channel and the t<sub>PLHD</sub> or t<sub>PHLD</sub> of the other channel on the same part.

Note 9:  $t_{SKD3}$  is the magnitude of the difference of any differential propagation delays between parts at the same V<sub>CC</sub> and within 5°C of each other.

Note 10: t<sub>SKD4</sub> is the magnitude of the difference of any differential propagation delays between parts operating over the rated supply and temperature ranges.

**Typical Operating Characteristics**  $(V_{CC} = 3.3V, V_{CM} = 1.2V, |V_{ID}| = 0.2V, f_{IN} = 200MHz, C_L = 15pF, T_A = +25^{\circ}C, unless otherwise specified.)$ 



MAX9171/MAX9172

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# MAX9171 Pin Description

Ρ	IN	NAME	FUNCTION
SOT23	SO/TDFN	NAME	FUNCTION
1	8	V <sub>CC</sub>	Positive Power-Supply Input. Bypass with a $0.1\mu F$ and a $0.001\mu F$ capacitor to GND with the smallest capacitor closest to the pin.
2	5	GND	Ground
3	7	OUT	Receiver Output
4, 5, 6	3, 4, 6	N.C.	No Connection. Not internally connected.
7	2	IN+	Noninverting Differential Receiver Input
8	1	IN-	Inverting Differential Receiver Input
—	(TDFN only)	EP	Exposed Paddle. Solder to PCB ground.

### \_MAX9172 Pin Description

P	IN	NAME	FUNCTION
SOT23	SO/TDFN	NAME	FUNCTION
1	8	V <sub>CC</sub>	Positive Power-Supply Input. Bypass with a $0.1\mu F$ and a $0.001\mu F$ capacitor to GND with the smallest capacitor closest to the pin.
2	5	GND	Ground
3	7	OUT1	Receiver Output 1
4	6	OUT2	Receiver Output 2
5	4	IN2-	Inverting Differential Receiver Input 2
6	3	IN2+	Noninverting Differential Receiver Input 2
7	2	IN1+	Noninverting Differential Receiver Input 1
8	1	IN1-	Inverting Differential Receiver Input 1
_	(TDFN only)	EP	Exposed Paddle. Solder to PCB ground.

# **Detailed Description**

#### **LVDS** Inputs

The MAX9171/MAX9172 feature LVDS inputs for interfacing high-speed digital circuitry. The LVDS interface standard is a signaling method intended for point-topoint communication over controlled-impedance media, as defined by the ANSI TIA/EIA-644 standards. The technology uses low-voltage signals to achieve fast transition times and minimize power dissipation and noise immunity. The MAX9171/MAX9172 convert LVDS

#### Table 1. Input-Output Function Table

INPUTS	OUTPUT
(IN_+) - (IN)	OUT_
≥ 0mV	High
≤ -100mV	Low
Open	High
Undriven short	High
Undriven parallel termination	High

signals to LVCMOS/LVTTL signals at rates in excess of 500Mbps. These devices are capable of detecting differential signals as low as 100mV and as high as 1.2V within a 0 to  $V_{CC}$  input voltage range. Table 1 is the input-output function table.

#### Fail-Safe

The MAX9171/MAX9172 fail-safe drives the receiver output high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without fail-safe, differential noise at the input may switch the receiver and appear as data to the receiving system. An open input occurs when a cable and termination are disconnected. An undriven, terminated input occurs when a cable is disconnected with the termination still connected across the receiver inputs or when the driver of a receiver is in high impedance. An undriven, shorted input can occur due to a shorted cable.





Figure 1. Input with In-Path Fail-Safe Network Equivalent Circuit



Figure 2. Propagation Delay and Transition Test Time Circuit

#### In-Path vs. Parallel Fail-Safe

The MAX9171/MAX9172 have in-path fail-safe that is compatible with in-path fail-safe receivers, such as the DS90LV018A and DS90LV028A. Refer to the MAX9111/MAX9113 data sheet for pin-compatible receivers with parallel fail-safe and lower jitter. Refer to the MAX9130 data sheet for a single LVDS receiver with parallel fail-safe in an SC70 package.

The MAX9171/MAX9172 with in-path fail-safe are designed with a +40mV input offset voltage, a 2.5µA current source between V<sub>CC</sub> and the noninverting input, and a 5µA current sink between the inverting input and ground (Figure 1). If the differential input is open, the 2.5µA current source pulls the input to V<sub>CC</sub> -0.7V and the 5µA source sink pulls the inverting input to ground, which drives the receiver output high. If the differential input is shorted or terminated with a typical value termination resistor, the +40mV offset drives the receiver output high. If the input is terminated and floating, the receiver output is driven high by the +40mV offset, and the 2:1 current sink to current source ratio (5µA:2.5µA) pulls the inputs to ground. This can be an advantage when switching between drivers on a multipoint bus because the change in common-mode voltage from ground to the typical driver offset voltage of 1.2V is not as much as the change from V<sub>CC</sub> to 1.2V (parallel fail-safe pulls the bus to  $V_{CC}$ ). Figure 2 shows the propagation delay and transition test time circuit and Figure 3 shows the propagation delay and transition test time waveforms.



Figure 3. Propagation Delay and Transition Time Waveforms

#### ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The receiver inputs of the MAX9171/MAX9172 have extra protection against static electricity. These pins are protected to  $\pm$ 13kV without damage. The structures withstand ESD during normal operation and when powered down.

The receiver inputs of these devices are characterized for protection to the limit of  $\pm 13$ kV using the Human Body Model.

#### Human Body Model

Figure 4a shows the Human Body Model, and Figure 4b shows the current waveform it generates when discharged into a low-impedance load. This model consists of a 100pF capacitor charged to the ESD test voltage, which is then discharged into the test device through a  $1.5k\Omega$  resistor.

## Applications Information

#### **Supply Bypassing**

Bypass V<sub>CC</sub> with high-frequency surface-mount ceramic  $0.1\mu$ F and  $0.001\mu$ F capacitors in parallel, as close to the device as possible, with the  $0.001\mu$ F capacitor closest to the device. For additional supply bypassing, place a  $10\mu$ F tantalum or ceramic capacitor at the point where power enters the circuit board.

#### **Differential Traces**

Input trace characteristics affect the performance of the MAX9171/MAX9172. Use controlled-impedance PCB traces to match the cable characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of traces.

Each channel's differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

#### **Cables and Connectors**

Transmission media typically have a controlled differential impedance of about  $100\Omega$ . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

#### Termination

The MAX9171/MAX9172 require an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance values may range between  $90\Omega$  to  $132\Omega$ , depending on the characteristic impedance of the transmission medium.

When using the MAX9171/MAX9172, minimize the distance between the input termination resistors and the MAX9171/MAX9172 receiver inputs. Use a single 1% surface-mount resistor.

#### **Board Layout**

For LVDS applications, a four-layer PCB that provides separate power, ground, LVDS signals, and output signals is recommended. Separate the input LVDS signals from the output signals to prevent crosstalk. Solder the exposed pad on the TDFN package to a pad connected to the PCB ground plane by a matrix of vias. Connecting the exposed pad is not a substitute for connecting the ground pin. Always connect pin 5 on the TDFN package to ground.



Figure 4a. Human Body ESD Test Modules



Figure 4b. Human Body Current Waveform

**Chip Information** 

TRANSISTOR COUNT: 624 PROCESS: CMOS



# \_Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



# \_Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



# Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



# **Package Information (continued)**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON	DIMENS	SIONS	PAC	KAGE VA	RIATI	ONS					
SYMBOL	MIN.	MAX.	PKG	. CODE	Ν	D2	E2	е	JEDEC SPEC	b	[(N/2)-1] x e
А	0.70	0.80	T633	3-2	6	1.50-0.10	2.30-0.10	0.95 BSC	MO229 / WEEA	0.40-0.05	1.90 REF
D	2.90	3.10	T833	3-2	8	1.50-0.10	2.30-0.10	0.65 BSC	MO229 / WEEC	0.30-0.05	1.95 REF
E	2.90	3.10	T833	3-3	8	1.50-0.10	2.30-0.10	0.65 BSC	MO229 / WEEC	0.30-0.05	1.95 REF
A1	0.00	0.05	T103	33-1	10	1.50-0.10	2.30-0.10	0.50 BSC	MO229 / WEED-3	0.25-0.05	2.00 REF
L	0.20	0.40	T103	33-2	10	1.50-0.10	2.30-0.10	0.50 BSC	MO229 / WEED-3	0.25-0.05	2.00 REF
k	0.25	MIN.	T143	33-1	14	1.70-0.10	2.30-0.10	0.40 BSC		0.20-0.05	2.40 REF
A2	0.20	REF.	T14:	33-2	14	1.70-0.10	2.30-0.10	0.40 BSC		0.20-0.05	2.40 REF
NOTES:											
1. ALL [ 2. COPL 3. WARF 4. PACK 5. DRAW 6. "N" I 7. NUME	ANARITY AGE SH AGE LEI ING CO S THE BER OF	shall Ngth/p Nforms Total N Leads	E IN mm. ANG NOT EXCEED T EXCEED 0.11 ACKAGE WIDTH TO JEDEC MU UMBER OF LE SHOWN ARE F CKAGE ORIENT	0.08 mr 0 mm. ARE CO 0229, EX ADS. OR REFE	m. INSID KCEP	ERED AS S T DIMENSIO CE ONLY.	NS "D2" AN		C(S). ND T1433-1 & T	1433–2.	

### **Revision History**

Pages changed at Rev 2: 1, 2, 3, 6, 8, 10, 11, 12

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